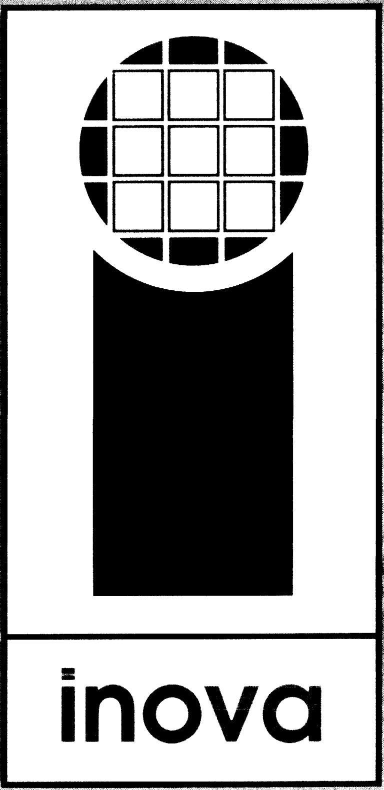
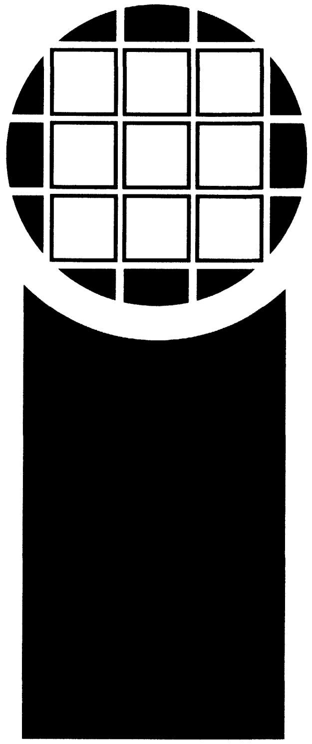


SRAM databook

high-speed, high-density monolithic SRAMs

inova
microelectronics
corporation

first edition
august 1990



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How To Use The Inova Databook

The Inova Databook has been designed to briefly introduce you to Inova, to familiarize you with our products, to provide you detailed specifications on our products, and to assist you in ordering the products that best suit your specific design requirements. The common thread throughout this effort has been YOU, our customers.

If you are unfamiliar with our company, a brief overview of our corporation is found on page 4.

If you would like to glance at the types of products Inova manufactures, please refer to the Product Selector Guide on page 11.

If you are trying to replace one or more of our competitors' parts with one of our high density monolithic devices, you may find the competitive device listed in our Cross Reference Section on page 17.

Once you have determined the correct device to use, the Product Data Section of the book will enable you to design it into your system correctly. Electrical and timing information is contained in this section, and the Packaging section at the rear of the book contains dimensions on all the packages we offer in our product line.

Memory Scale, a new memory performance comparison factor which is defined as the total number of memory bits divided by the device access time, is included for each Inova device. We encourage you to compare the Memory Scale number of competitive memory products with Inova memories.

A Quality and Reliability section outlines the system of controls we maintain to provide you with the highest quality and most reliable products and services. This section is found on page 21.

Several Application Notes on using Inova products are in the back of the book. These may help you consider different alternatives in your design with Inova devices.

Ordering information is included at the end of each individual data sheet and on pages 9 and 150.

Inova has the talent and the products to help you design superior advanced electronic systems that will help keep you a step ahead of your competitors. We look forward to hearing from you.

Inova Overview

Inova Microelectronics Corporation designs, produces and markets high density, high speed memory and special purpose semiconductor devices. Our headquarters in Santa Clara, California is augmented by our research and development and marketing group located in Colorado Springs, Colorado.

Inova has developed Inroute™, a proprietary technology that enables Inova to economically produce semiconductor devices on relatively large areas of silicon. This technology, when combined with our high speed silicon processing and design talents, has placed and will continue to maintain Inova in the forefront of semiconductor memory technology.

Inova subcontracts its wafer fabrication activities to silicon foundries worldwide to ensure a reliable large volume of manufacturing capacity. Since some of our products have been specified on Standardized Military Drawings which require MIL-STD-883C screening and controls, the rest of our products benefit from this influence.

Inova products include 256K and 1M monolithic memory devices available in a variety of widths, with a 4M monolithic device available soon. A high speed cache memory, a neural network chip and other specialized memory devices are also in the works. Inova will continue to provide semiconductor devices designed to solve industry-wide and customer- unique requirements.

Letter from the President

Dear Reader,

We would like to thank you for considering **Inova** for your static random access memory needs. It is our objective to make you a satisfied customer by solving your needs with our products and services.

The world's first production-released monolithic 1-Megabit static RAM, the S128K8, was from **Inova**. The S128K8 device has been in production for over two years now, and was the first monolithic 128Kx8 SRAM available on a Standardized Military Drawing. Having established that leadership, we are committed to staying at the forefront of high density memory technology. During 1990, we will continue our pioneering with the introduction of our four and sixteen megabit SRAM's, as well as other highly sophisticated special application memory products.

Although our products are what formally generates revenue to further our business, our people create the products that address your needs as a customer. We would appreciate your feedback on the devices we have designed that appear in this databook. Feel free to contact any of us to obtain more information on our products, or to discuss your particular design challenges and how we might better serve your needs.

We would like to be your memory supplier, and we appreciate the consideration you have given us by reviewing our databook. When you determine the correct **Inova** product to satisfy your needs, contact your local sales representative, distributor, or our Customer Service department to place your order!

Vaemond H. Crane

President

Important Notice

Inova guarantees that its circuits will be free from defects in materials and workmanship under normal use and service when operated under recommended operating conditions, and that these circuits will perform to current specifications in force at the time of their manufacture. Inova backs its devices with the Inova standard warranty which is detailed on the reverse of the Inova sales order acknowledgement. Testing and other quality control techniques are utilized to the extent Inova deems necessary to support this warranty. Unless mandated by specific purchase order terms or required by military specifications, testing of all parameters of each device is not necessarily performed. Inova assumes no responsibility for the use of any circuits described in this databook, and does not convey any license under its patent rights or the rights of others.

The information presented in this databook is accurate to the best of our knowledge. Inova reserves the right to make changes in the device specifications to improve manufacturability, reliability, or performance, or to change the availability of the devices themselves at any time without notice. Inova assumes no responsibility for any errors or ommissions in this book, updates to this databook, or for applications assistance or customer product designs.

Inova products are not authorized for use as critical components in life support devices or systems intended for surgical implant in the body without express written consent of the president of Inova Microelectronics Corporation. Buyer agrees to notify Inova of any such intended end use whereupon Inova shall determine the suitability and availablity of such use.

Table of Contents

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Ordering Information

S 128K 8 TL-45MC

C = 600 mil ceramic sidebrazed DIP
D = 400 mil CERDIP
E = 400 mil ceramic sidebrazed DIP
T = 300 mil ceramic sidebrazed DIP
P = 400 mil Plastic DIP
F = Flatpack
S = Ceramic SOJ
J = Plastic SOJ
L= Leadless chip carrier
G= Pin Grid Array

M = Military Temp (-55°C to +125°C)
I = Industrial Temp (-40°C to +85°C)
C = Commercial Temp (-0°C to +70°C)

Speed or frequency

L = Low Power
Blank = Standard Power

T = Two Chip Selects
Blank = One Chip Select

Memory width, in bits*

Memory Depth, in bits*

S = SRAM

C = Cache

*or another unique circuit designator

Product Selector Guide

32K x 8 bit SRAMs

Inova	Access Time	Packages		Temp		
Part Number	ns Max	Type	Pins	Range	Comments	Page
S32K8	55, 70, 85, 100	C, L	28	C, I, M	DESC SMD No. 5962-88662	43
S32K8L	55, 70, 85, 100	C, L	28	C, I, M	DESC SMD No. 5962-88552	43

C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (-40°C to 85°C)
M = Military Temperature Range (-55°C to 125°C)

L suffix on base part number = Low Power Device
T suffix on base part number = Two Chip Select Option

C = 600 mil Ceramic Sidebrazed DIP
D = 400 mil CERDIP
E = 400 mil Ceramic Sidebrazed DIP
T = 300 mil Ceramic Sidebrazed DIP
P = 400 mil Plastic DIP
F = Flatpack
S = Ceramic SOJ
J = Plastic SOJ
L = Leadless Chip Carrier
G = Pin Grid Array

128K x 8 bit SRAMs

Inova Part Number	Access Time ns Max	Packages Type	 Pins	Temp Range	Comments	Page
S128K8	25, 35, 45 55, 70, 85 100, 120	C, D, E, T, F S, L, J, P	32	C, I, M	25 ns commercial only	49
S128K8L	25, 35, 45, 55, 70, 85 100, 120	C, D, E, T, F S, L, J, P	32	C, I, M	DESC SMD No. 5962-89598 25 ns commercial only	49
S128K8T	25, 35, 45, 55, 70, 85 100, 120	C, D, E, T, F S, L, J, P	32	C, I, M	25 ns commercial only	57
S128K8TL	25, 35, 45, 55, 70, 85 100, 120	C, D, E, T, F S, L, J, P	32	C, I, M	25 ns commercial only	57

C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (-40°C to 85°C)
M = Military Temperature Range (-55°C to 125°C)

L suffix on base part number = Low Power Device
T suffix on base part number = Two Chip Select Option

C = 600 mil Ceramic Sidebrazed DIP
D = 400 mil CERDIP
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T = 300 mil Ceramic Sidebrazed DIP
P = 400 mil Plastic DIP
F = Flatpack
S = Ceramic SOJ
J = Plastic SOJ
L = Leadless Chip Carrier
G = Pin Grid Array

64K x 16 bit SRAMs

Inova Part Number	Access Time ns Max	Packages Type	Pins	Temp Range	Comments	Page
S64K16	45, 55, 70, 85, 100, 120	C	40	C, I, M	DESC SMD No. 5962-90858	65
S64K16L	45, 55, 70, 85, 100, 120	C	40	C, I, M	DESC SMD No. 5962-90858	65

256K x 4 bit SRAMs

Inova Part Number	Access Time ns Max	Packages Type	Pins	Temp Range	Comments	Page
S256K4	25, 35, 45	C, E, P, F, S J, L, T	28	C, I, M	Preliminary	71
S256K4L	25, 35, 45	C, E, P, F, S J, L, T	28	COM	Preliminary	71

1,024K x 1 bit SRAMs

Inova Part Number	Access Time ns Max	Packages Type	Pins	Temp Range	Comments	Page
S1M1	25, 35, 45	C, E, P, F, S J, L, T	28	C, I, M	Preliminary	79
S1M1L	25, 35, 45	C, E, P, F, S J, L, T	28	C, I, M	Preliminary	79

512K x 8 bit SRAMs

Inova	Access Time	Packages		Temp		
Part Number	**ns Max**	**Type**	**Pins**	**Range**	**Comments**	**Page**
S512K8	45, 55, 70	C	32	C, I, M	Preliminary	87
S512K8L	45, 55, 70	C	32	C, I, M	Preliminary	87

256K x 16 bit SRAMs

Inova	Access Time	Packages		Temp		
Part Number	**ns Max**	**Type**	**Pins**	**Range**	**Comments**	**Page**
S256K16	55, 70, 85, 100, 120	C	48	C, I, M	Advance Information	93
S256K16L	55, 70, 85, 100, 120	C	48	C, I, M	Advance Information	93

C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (-40°C to 85°C)
M = Military Temperature Range (-55°C to 125°C)

L suffix on base part number = Low Power Device
T suffix on base part number = Two Chip Select Option

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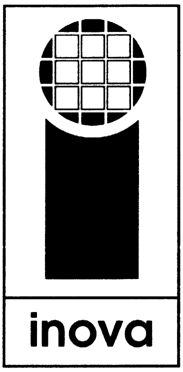
D = 400 mil CERDIP
E = 400 mil Ceramic Sidebrazed DIP
T = 300 mil Ceramic Sidebrazed DIP
P = 400 mil Plastic DIP
F = Flatpack
S = Ceramic SOJ
J = Plastic SOJ
L = Leadless Chip Carrier
G = Pin Grid Array

Cross References



32K x 8

55 nS

Competition	Inova
CY7C198	S32K8-55
CY7C199	(p. 43)
IDT71256S	
IDT7M856	
SRM22256C	
KM68257	
CXK58258	
LH52256	

70 nS

Competition	Inova
CXK58257SP	S32K8-70
IDT71256S	(p. 43)
IDT7M856	
M5M5256A	
SRM22256C	
LH52256	
DPS92256	
EDI8832C	

85 nS

Competition	Inova
HM62256	S32K8-85
CXK58257M	(p. 43)
SSI62256CD	
IDT71256S	
IDT7M856	
GM76C256L	
EDH8832C	
EDI8832C	

32K x 8

100 nS

Competition	Inova
MB84256A	S32K8-100
GM76C256	(p. 43)
CDM62256	
HM62256	
HY63C256	
SRM20256C	
LC36256L	
CXK58257P	
UM62256	

128K X 8

25 nS

Competition	Inova
MT5C1008	S128K8-25
	(p. 49)

35 nS

Competition	Inova
CXK581020	S128K8-35
MT5C1008	(p. 49)
DPS41288	

45 nS

Competition	Inova
CXK581020	S128K8-45
MSM8128	(p. 49)

55 nS

Competition	Inova
CXK581020	S128K8-55
MSM8128	(p. 49)
IDT8M824	

128K X 8

70 nS

Competition	Inova
EDI8M8128	S128K8-70
EDI88128	(p. 49)
CXK581001	
DPS128M8	
HM628128	
MSM8128	
IDT8M824	
EDI88130	S128K8T-70
	(p.57)

85 nS

Competition	Inova
CXK581001	S128K8-85
DPS128M8	(p. 49)
EDI88128	
M5M51008	
SRM20100	
MSM8128	
HM658128	
HM628128	
IDT8M824	
EDI88130	S128K8T
	(p. 57)

100 nS

Competition	Inova
EDI88128	S128K8-100
HM658128	(p. 49)
MSM8128	
CXK581000	
SRM20100	
M5M51008	
MS88128	
MS12808	
IDT8M824	
EDI88130	S128K8T-100
	(p. 57)

128K X 8

120 nS

Competition	Inova
DPS128M8	S128K8-120
EDI8M8128	(p. 49)
EDI88128	
HM658128	
MS12808	
CXK581000	
M5M51008	
MSM8128	
EDI88130	S128K8T-120
	(p. 57)

64K x 16

45 nS

Competition	Inova
IDT8M624	S64K16-45
DPS8M624	(p.65)

55 nS

Competition	Inova
EDH816H64	S64K16-55
EDI8M1664	(p.65)
DPS8M624	
IDT8M624	

70 nS

Competition	Inova
EDH816H64	S64K16-70
CYM1623	(p.65)
DPS8M624	

100 nS

Competition	Inova
EDH816H64	S64K16-100
EDI8F1664	(p.65)
DPS8M624	

256K x 4

25 nS

Competition	Inova
431004	S256K4-25
M5M51004	(p. 71)
MT5C1005	
CYM1240	
EDI8M4257	

35 nS

Competition	Inova
EDI84256	S256K4-35
EDI8M4257	(p. 71)
M5M51004	
MT5C1005	
HM624256	
VT624256	
IDT7M4042	

45 nS

Competition	Inova
MSM4256	S256K4-45
M5M51004	(p. 71)
HM624256	
VT624256	
EDI84256	
EDI8M4257	
IDT7M4042	

1M X 1

25 nS

Competition	Inova
M5M51001	S1M1-25
MT5C1001	(p. 79)
431001	

35 nS

Competition	Inova
M5M51001	S1M1-35
MT5C1001	(p. 79)
EDI811024	

45 nS

Competition	Inova
M5M51001	S1M1-45
EDI811024	(p. 79)
MSM11000	

512K x 8

45 nS

Competition	Inova
CYM1464	S512K8-45
IDT7MB4048	(p. 87)

70 nS

Competition	Inova
DPS512X8	S512K8-70
IDT7M4048	(p. 87)

256K x 16

55, 70 nS

Competition	Inova
EDI8M16256	S256K16
	(p. 93)

Quality and Reliability

inova

QUALITY & RELIABILITY
OUR COMMITMENT TO SUPERIOR PRODUCT QUALITY

Inova is committed to excellence in product quality and reliability. Stringent controls are in place in all phases of product design and throughout manufacturing to achieve our goals. However, the only true measurement of that commitment is our customer's satisfaction. Our customers are our most important "Quality Monitor" and **Inova** is most responsive to their inputs.

There are six critical factors that are essential for **Inova** to achieve excellence in Quality and Reliability. They are:

1. A deep understanding of our customers' needs and wants that translates into useful products.

2. Long lasting relationships with customers going beyond the delivery of the product to include sales, service, and ease of use.

3. Close partnerships with suppliers and customers who feed suggestions for improvements back into our operations.

4. A commitment that runs from the top to the bottom of the organization to continuously improve the yield, quality, and reliability of our products.

5. A system for measuring these improvements accurately.

6. A focus on prevention of mistakes rather than correcting them.

A description of the systems and controls in place at **Inova** which assure that the highest quality parts are consistently supplied and that these parts have the highest reliability achievable follows. We are always happy to explain our quality and reliability programs in more detail in person.

QUALITY ASSURANCE METHODS

CUSTOMER INFORMATION

Inova Microelectronics Corporation exists to satisfy customers' needs with high performance, high density semiconductor products. To succeed in this endeavor, our sales and marketing team must understand our customers thoroughly and communicate our customers' needs back to our organization effectively.

Once a customer's need is identified and can be solved by **Inova**, a product purchase is normally transacted. **Inova**'s commitment as a result of this purchase order does not terminate with the delivery of the product, but includes technical service and a healthy exchange of information to ensure that the device is easy for the customer to use. Suggestions from our customers on ways to improve our products, systems, and services are actively solicited from the entire **Inova** organization.

The quality of our organization is measured not only by the acceptability of our products, but by how our entire organization responds to our customers' needs.

CUSTOMER-SPECIFIC DRAWINGS

Drawings and specifications received from customers and agreed to by **Inova** are controlled by the marketing department. When revisions occur they are reviewed and agreed to as if they were new specifications. Inova generates an internal specification that is used to manufacture any product that is not "standard". The Quality department controls these customer specifications. While **Inova** encourages standardization and makes every effort to create a device that will satisfy the majority of customer needs, we do realize that customer requirements sometimes do not match our datasheet parts.

SUPPLIER COMMUNICATIONS

Potential suppliers are initially evaluated by Inova engineering and quality assurance departments to determine the viability of the supplier. Once the supplier is deemed viable by passing an exhaustive technical analysis, he is added to the Inova Approved Suppliers list. This list is maintained by both Engineering and Quality and only those suppliers on the list are used.

Inova controls are imposed on all our raw material suppliers. Procurement specifications are written to cover our requirements. These specifications are always referenced in the purchase orders placed with our suppliers and a copy is attached for reference.

Inova suppliers enjoy the same type of continuous communications that we strive to maintain with our customers. This constant dialogue ensures that timely improvements are made in both organizations to maximize the useful benefits of our customer/supplier relationships.

YIELD IMPROVEMENT

Inova is driven by constant yield improvement. Since there are a set number of die sites on a silicon wafer, **Inova's** goal is to continually drive process and design improvements to achieve the highest percentage of die sites producing good product. There is no higher priority in the product engineering department. Achieving high yields has a direct effect on the "cost of quality".

Inova spends a large proportion of its resources on yield improvement as a preventive measure in quality, rather than on inspection and rework as an inspection and failure detection measure. This constant perfecting of the product during the course of its lifetime assures a better part in terms of quality, reliability and costs as time goes by. This is the classic microelectronic "learning curve". Because of **Inova**'s proprietary Inroute™ technology, this objective is realized much earlier in **Inova**'s product life cycle.

DOCUMENTATION AND CONTROL OF MANUFACTURING

Inova Quality Assurance maintains a documentation system which covers the design, wafer fabrication, assembly, test, quality assurance, reliability, and marketing areas of our company. Device schematics & drawings for all piece parts are under document control. All materials used in the manufacture of **Inova** products are covered by material specifications. Sign-off approvals for all standard product manufacturing and procurement specifications are pre-defined and only approved specifications are used for procurement and production.

Original customer drawings are kept on file by **Inova** Marketing. When a customer's need can best be met by a special version of an **Inova** device, the customer's requirements are translated into a unique **Inova** internal specification that describes exactly how the part is built, tested and marked. This internal document eliminates any misunderstandings that may be introduced by directly using customer specifications.

A revision control system is in effect for all schematics, drawings, and materials specifications. Each revision of a specification has an effectivity date and copies of all past revisions are kept on file and traceable.

PRODUCT CHANGE CONTROL

Changes to the design, materials, or process of an **Inova** product are thoroughly evaluated and qualified before being implemented. Product characterization and reliability tests are performed based on the type of change made.

Changes that affect device operation or interchangeability are communicated to customers with sufficient time to allow for the customer's evaluation and acceptance.

Changes to Military products are communicated to the qualifying activity.

IN-PROCESS MONITORS AND INSPECTIONS

While the basic philosophy at **Inova** is to "Do it right the first time", constant vigilance is required to verify the quality of our products and procedures. An extensive system of monitors and inspections are performed in the manufacturing and testing of our products. Information from these inspections is summarized for the management of the respective areas and for the general management team and corrective action is implemented when required to improve performance. To emphasize the importance of quality to the overall success of the company, quality measurement is used as one of the criteria in the assessment of **Inova** management's performance.

Because of our commitment to produce the most reliable product available for commercial, industrial and military OEMs, many of the inspection procedures for **Inova** product are based on MIL-STD-883, Revision C. We have found it easier and more cost effective to implement the most stringent military standards required for our devices and reap the benefits of those higher standards in our commercial products.

INCOMING INSPECTION OF PURCHASED MATERIALS

All materials purchased for use in the manufacture of **Inova** products are inspected before their actual use. Only approved and accepted product is used in production. Material that is rejected is returned to the vendor for corrective action.

Inova encourages partnership arrangements and open dialogue with all suppliers of **Inova** raw materials. Swift resolution of problems and the highest levels of quality are sought with all suppliers. **Inova** vendors are measured by their failure rate and willingness to solve problems should they occur. Excessive failures or a lack of cooperation leads to a vendor disqualification.

STATISTICAL PROCESS CONTROL

Statistical Process Control, or SPC, is a system of defect prevention through the application of statistical tools. These tools are used on data taken at critical process points in the manufacturing flow and provide insight into the manufacturing process itself. When the results are interpreted correctly, SPC provides opportunities for improvement in the overall manufacturing process. By the proper application of SPC, process variation is reduced and a more consistent and reliable product is manufactured.

Inova uses extensive SPC techniques in the analysis of wafer fabrication, assembly and test process parameters. All **Inova** manufacturing operations have SPC systems in place. Diffusion, implant, masking, gate oxidation, die attach, & wire bonding are just a few examples of manufacturing process points monitored.

AUDIT AND CORRECTIVE ACTION

In order to verify compliance to requirements, audits of all **Inova** manufacturing and quality control areas are carried out at least once per year. These audits are conducted by the Quality Assurance organization and records of each audit are kept on file. All discrepancies found on the audit result in a corrective action request. All corrective actions must be implemented and approved by the auditor before they are closed out. Pre-defined checklists are used for all audits and they are kept under document control.

TRAINING AND CERTIFICATION

All critical processes and inspections are performed by personnel who have been trained to perform their task in accordance with **Inova** requirements. Each person is trained and tested by a qualified individual to assure proficiency at the task. Individuals are retested periodically to verify proficiency.

CALIBRATION

All equipment used for measuring and testing of product is calibrated on an assigned schedule utilizing equipment and standards traceable to the National Bureau of Standards. The Quality Assurance group maintains the calibration of measuring equipment.

The calibration system is set up to comply with MIL-STD-45662. All manufactured products are measured and/or tested by equipment that has been properly calibrated on pre-defined schedule. Automatic testers, temperature forcing units, dimensional measurement tools, and electronic instruments of all types are examples of the types of equipment that **Inova** calibrates and maintains.

ELECTROSTATIC DISCHARGE (ESD) PREVENTION

Inova has a complete electrostatic discharge (ESD) prevention program to prevent any ESD damage from occurring during the manufacturing process. This system is in full conformance with JEDEC Publication No. 108-A. Ground straps, grounded table tops, smocks, and grounded equipment are all utilized. All personnel are trained to prevent ESD damage. Parts are packed for shipment in ESD protective packaging. All ESD safeguards are checked periodically to verify grounds and connections.

All **Inova** devices are designed with protection networks on inputs and outputs to assure adequate protection from normal ESD damage. New designs are thoroughly tested prior to release to assure sufficient levels of ESD protection. ESD acceptance tests are conducted per MIL-STD-883C, method 3015.

CUSTOMER RETURNS & FAILURE ANALYSIS

Even using the most extensive quality assurance and reliability techniques, product failures may occur in the field. Field failures are given the highest priority for failure analysis and feedback. **Inova** parts which are returned are analyzed to determine the root cause of the problem. All failure analysis information is communicated directly to the customer by **Inova**. If changes are made by **Inova** to the testing or the manufacturing flow of a product to correct a problem then the effective date code of the change is also communicated to the customer.

Inova maintains a state-of-the-art failure analysis lab. Our failure analysis equipment includes a Scanning Electron Microscope (SEM), a Wafer Parametric Tester, and various electronic failure verification and fault isolation tools. All quality conformance and field failures are thoroughly analyzed to determine the cause of the failure and corrective action. Yield-related failures are analyzed to determine actions neccessary to improve manufacturing yields. An in-depth failure analysis is essential to improve the yield, quality and reliability of **Inova** products.

SUMMARY

Inova is committed to supplying the highest quality, most reliable semiconductor products available in the industry. We strive to solve our customers need with our products and our people, but can be most successful if we maintain a high level of communication with you, our customer, and our suppliers.

If you have a suggestion to help improve any of our products or systems, please contact us. We definitely want to be your Number 1 supplier of semiconductor products.

RELIABILITY

DESIGN

At **Inova**, building high quality, highly reliable microcircuits is no accident. We start with the product design itself. No reliability program can be successful without the design and process engineering team understanding exactly what the reliability goals of a particular design project are and what design and process considerations must be made to achieve those goals.

The wafer fab process is **Inova**'s first reliability consideration. The fabrication process must be fully characterized and proven using known test structures to measure individual device performance and reliability. Once the process parameters and the design rules are documented, the circuit designer can begin to design the microcircuit.

Other reliability considerations during the device design process include ESD protection networks and latch-up protection. **Inova** uses very conservative design margin simulations to assure that new products perform well within the specification limits.

The next area of concern in device design is the assembly of the finished good die. Packaging design rules are followed to assure that assembly manufacturing tolerances are observed.

Inova knows that to be competitive in the world market in the 1990's and beyond, we must design for optimum manufacturing capability. Inova designers work closely with production engineers to make sure that new designs are optimized for manufacturing. This is an extremely important consideration that produces dramatic benefits with new **Inova** products as they ramp up in production.

CHARACTERIZATION & QUALIFICATION TESTING

Once an **Inova** microcircuit is designed and produced, it must be characterized and qualified. The characterization of a new **Inova** design is extremely important to verify that the performance meets the design goals and the device specification. Three wafer fab lots are required for characterization to assure consistency of the process and design. Extensive tests are done at this stage to verify that the new product will meet all performance goals. Thorough characterization assures that **Inova** microcircuits will perform in all possible applications and under all conceivable conditions.

Qualification tests are done to verify the long term reliability of the device under all conceivable conditions. These tests are designed to accelerate failures whenever possible to allow for relatively short duration tests which can still accurately predict longer term failure rates. Reliability tests are divided into "die related" tests and "package related" tests. The tests that **Inova** performs are described below:

PACKAGE RELATED TESTS

TEST	***CONDITIONS***	***SAMPLE SIZE***	***MAX % FAIL****
MARK PERM	MIL-STD-883C, Method 2015	4	0
SOLDER-ABILITY	MIL-STD-883C, Method 2003 (# OF LEADS TESTED)	84	LTPD = 10
BOND STRENGTH	MIL-STD-883C, Method 2011 (# OF LEADS TESTED)	60	LTPD = 15
PHYSICAL DIMENSIONS	MIL-STD-883C, Method 2016	15	0
LEAD INTEGRITY	MIL-STD-883C, Method 2004 Condition B2	15	0
INTERNAL WATER VAP.	MIL-STD-883C, Method 1018 (<5000PPM)	5	1/5
ADHESION OF LEAD FINISH	MIL-STD-883C, Method 2025	15	0
LID TORQUE	MIL-STD-883C, Method 2024	5	0

* Maximum percentage of failures allowed by MIL-STD-883C.

SERIES 1

TEST	CONDITIONS	SAMPLE SIZE	MAX % FAIL*
THERMAL SHOCK	MIL-STD-883C, Method 1011 Condition B, 15 CYCLES	15	0
TEMP CYCLE COND C,	MIL-STD-883C, Method 1010 100 CYCLES	15	0
FINE/GROSS LEAK	MIL-STD-883C, Method 1014	15	0
VISUAL	MIL-STD-883C	15	0
TEST ENDPOINT	PER DATA SHEET AT ROOM, HOT, & COLD TEMP.	15	0

* Maximum percentage of failures allowed by MIL-STD-883C.

DIE RELIABILITY TESTS

TEST	CONDITIONS	SAMPLE SIZE	MAX % FAIL*
INFANT MORTALITY	168 hours/125°C or equivalent	100	1%
LIFE TEST	1000 hours/125°C or equivalent	100	1%
TEMP CYCLE	100 CYCLES -65/+150°C	50	2%

* Maximum percentage of failures allowed by MIL-STD-883C.

DIE PERFORMANCE TESTS

TEST	*CONDITIONS*	*SAMPLE SIZE*	*MIL SPEC**	*INOVA SPEC*
ESD SENSITIVITY	MIL-STD-883C, Method 3015 (Human Body Model)	3	> 1000V	> 2000V
LATCH-UP	INOVA Specification TE-0201	5	0	0

* Maximum percentage of failures allowed by MIL-STD-883C.

These tests are performed on each new **Inova** design. Changes made to existing designs to improve performance or increase manufacturing yields are also requalified. Whenever a change is made, Inova analyzes it to determine its possible effect on device performance or reliability. All changes that may have an effect on device performance or reliability are recharacterized and requalified before they are put into production. Because some **Inova** customers require notification and requalification at their facility before a redesigned product may be supplied, **Inova** policy requires us to notify those customers well in advance of major changes in the design to allow time for requalification, if necessary.

MILITARY PRODUCTS

Inova is a major supplier of Military Static RAMs to the U.S. Government and to its prime and subcontractors. The ability to supply this level of high reliability product requires **Inova** to have the quality systems in place to meet the requirements of MIL-STD-883C, Paragraph 1.2.1, and the referenced paragraphs of MIL-M-38510.

In addition to these military specifications, **Inova** complies with other associated Quality System specifications, such as MIL-Q-9858A & MIL-I-45208A. **Inova** processes all military product through the screening flow of MIL-STD-883C, Method 5004, Class B. Quality Conformance Inspection (QCI) testing is performed per MIL-STD-883C, Method 5005, Class B. A description of **Inova**'s screening and QCI testing follows.

SCREENING FLOW

Requirement	*Inova Specification or MIL-STD-883C Test Method*
Internal Visual Inspection	Method 2010, Condition B
Temperature Cycling	Method 1010, Condition C (50 cycles)
Constant Acceleration	Method 2001, Condition D, Y1 Only
External Visual Inspection	Para. 3.2 of Method 1010
Initial Electrical Test	TE - 0202
Burn-in	Method 1015, Condition D 80 Hrs @ 150° C.
Final Electrical Test (Note 1)	TE - 0202, 25° C

Requirement	***Inova Specification or MIL-STD-883 Test Method***
Percent Defective Allowable	< 3%
Final Electrical Test	TE - 0202, +125°/-55°
Mark	AS - 0402
Group A Test @+125°/-55° C	TE - 0202
Hermeticity, Fine & Gross Leak	Method 1014
Group A Test @ 25° C	TE - 0202
External Visual Examination	QA - 0302
Pack	QA - 0202
Final QA	QA - 0201
Ship	QA - 0202

Note 1: Parts must be tested @ 25° C within 96 hours of removal from burn-in.

QUALITY CONFORMANCE TESTING

Quality conformance testing follows the requirements contained in MIL-STD-883C, paragraph 1.2.1 (17). Group A and B tests are required on every inspection lot and Group C and D tests are done as required by MIL-M-38510.

MIL-STD-883C and Inova Specifications

GROUP A TESTS

TEST	***DESCRIPTION***	***(ACC/SS) OR LTPD***
Subgroup 1	Static Tests @ +25° C.	0/116
Subgroup 2	Static Tests @ +125° C.	0/116
Subgroup 3	Static Tests @ -55° C.	0/116
Subgroup 7	Functional Tests @ +25° C.	0/116
Subgroup 8A	Functional Tests @ +125° C.	0/116
Subgroup 8B	Functional Tests @ -55° C.	0/116
Subgroup 9	Switching Tests @ +25° C.	0/116
Subgroup 10	Switching Tests @ +125° C.	0/116
Subgroup 11	Switching Tests @ -55° C.	0/116

GROUP B TESTS

TEST	***DESCRIPTION***	***(ACC/SS) OR LTPD***
Subgroup 2	Resistance to solvents, MIL-STD-883C, Method 2015	0/4
Subgroup 3	Solderability, MIL-STD-883C, Method 2003	10
Subgroup 4	Bond Strength, MIL-STD-883C, Method 2011, Cond. D	10

GROUP C TESTS

TEST	DESCRIPTION	(ACC/SS) OR LTPD
Subgroup 1	Steady State Life Test MIL-STD-883C, Method 1005, Condition D 184 hrs @ 150° C	5
	End Point Electrical Parameters Subgroups 2, 3, 7, & 8	5

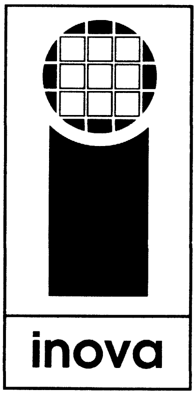
GROUP D TESTS

TEST	DESCRIPTION	(ACC/SS) OR LTPD
Subgroup 1	Physical Dimensions, MIL-STD-883C, Method 2016	15
Subgroup 2	Lead Integrity, MIL-STD-883C, Method 2004, Condition B_2 (lead fatigue)	15
Subgroup 3	Thermal Shock, MIL-STD-883C, Method 1011, Condition B, 15 cycles	15
	Temperature Cycling, MIL-STD-883C, Method 1010, Condition C, 100 cycles	15
	Moisture Resistance, MIL-STD-883C, Method 1004	15
	Fine & Gross Leak Test, MIL-STD-883C, Method 1014	15
	Visual Inspection, MIL-STD-883C	15
	End Point Electrical Parameters Subgroups 2, 3, 7, & 8	15
Subgroup 4	Mechanical Shock, MIL-STD-883C, Method 2002, Condition B	15
	Vibration, Variable Frequency, MIL-STD-883C, Method 2007, Condition A	15
	Constant Acceleration, MIL-STD-883C, Method 2001, Condition D (20KG), Y_1 orientation	15
	Fine & Gross Leak Test, MIL-STD-883C, Method 1014	15

GROUP D TESTS (cont'd)

TEST	DESCRIPTION	(ACC/SS) OR LTPD
Subgroup 4, (cont'd)	Visual Inspection, MIL-STD-883C	15
	End Point Electrical Parameters Subgroups 2, 3, 7, & 8	15
Subgroup 5	Salt Atmosphere, MIL-STD-883C, Method 1009, Condition A	0/15
	Visual Inspection, MIL-STD-883C	0/15
	Fine & Gross Leak Test, MIL-STD-883C, Method 1014	0/15
Subgroup 6	Internal Water Vapor Content, MIL-STD-883C, Method 1018, (< 5000ppm)	0/3
Subgroup 7	Adhesion of Lead Finish, MIL-STD-883C, Method 2025	0/15
Subgroup 8	Lid Torque, MIL-STD-883C, Method 2024	0/5

Product Data



inova microelectronics

inova

S32K8

Product Data

32K x 8 Static RAM

Key Parameters	***Device Types***				
S32K8 and S32K8L	***55I 55C***	***70M 70I 70C***	***85M 85I 85C***	***100M 100I***	***Unit***
Access Time	55	70	85	100	nS
Cycle Time	55	70	85	100	nS
Output Enable Access	20	25	30	50	nS

Features

- **S32K8L is compliant to DESC Standardized Military Drawing 5962-88552 (Standard power part compliant to 5962-88662)**
- **2.0V Low-Power Data Retention Option (S32K8L)**
- **Military, industrial, and commercial temperature range**
- **Military grades compliant to MIL-STD-883C**
- **28 pin JEDEC standard pinout**

General Description

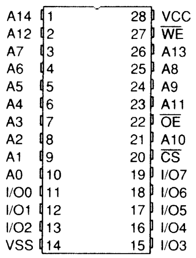
The Inova S32K8 is a high performance 256K bit Static Random Access Memory (SRAM), organized as 32K eight bit bytes.

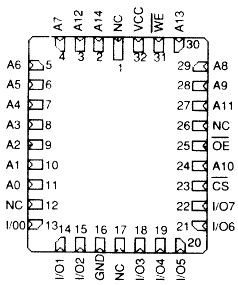
The S32K8 is manufactured using a highly reliable, four transistor cell CMOS process. This provides a component which combines low active and standby power characteristics with high performance.

All inputs and outputs are fully TTL compatible. Operation is fully static, so there is no need for extra control logic to generate clocks and timing strobes.

Every military grade device is fully compliant to MIL-STD-883C, paragraph 1.2.1. Industrial and commercial grade devices are produced in the same production line which ensures that they are also of the highest quality.

Package Options





A0-A14	Address Inputs
I/O0-I/O7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V Power
V_{SS}	Ground

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage(1)	V_{CC}	4.5	5.5	V
Input HIGH Voltage	V_{IH}	2.2	V_{CC}+0.5	V
Input LOW Voltage	V_{IL}	-0.5	0.8	V
Operating Temp. Mil.	T_C	-55	125	°C
Operating Temp. Ind.	T_C	-40	85	°C
Operating Temp. Comm.	T_C	0	70	°C

Absolute Maximum Ratings (2)

Temperature Under Bias	-55 °C to 125 °C
Storage Temperature	-65 °C to 150 °C
Supply Voltage(1)	-0.5V to 7.0 V
Signal Voltage On Any Pin	-0.5 V to V_{CC} + 0.5V
Power Dissipation	1 Watt
D.C. Continuous Output Current Per Output	20 mA
Lead Temperature (Soldering 10 sec)	260 °C

Notes:

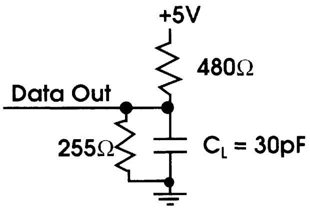
1. All voltages referenced to V_{SS} (GND).

2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	High Z	I_{SB}/I_{FSB}
Read	L	L	H	Output	I_{CC2}
Write	L	X	L	Input	I_{CC2}
Output Disable	L	H	H	High Z	I_{CC2}

Load Test Circuits



C_L = 5pF for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{WLZ}.

Memory Scale

Access Time	55	70	85	100	Unit
S32K8	4.7	3.7	3.0	2.6	kbits/ns

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

DC and Operating Characteristics

M=Military; C=Commercial; I=Industrial

Parameters	Symbol	Test Conditions		S32K8		S32K8L			UNITS
				Min	Max	Min	TYP 5V, 25°C	Max	
Input Leakage	$\lvert I_{LI} \rvert$	V_{CC} = max, V_{IN} = GND to V_{CC}			2			2	µA
Output Leakage	$\lvert I_{LO} \rvert$	V_{OUT} = GND TO V_{CC}, $\overline{CS} \geq V_{IH}$			2			2	µA
Static Supply Current	I_{CC1}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$ No Address Transitions	C		80		55	80	mA
			I		85			85	
			M		90			90	
Dynamic Supply Current	I_{CC2}	$\overline{CS} \leq V_{IL}$, $\overline{OE} = V_{IH}$ Address Change every t_{RC}	55		110		95	110	mA
			70,85,100		100		90	100	
Standby Supply Current with TTL Inputs	I_{SB}	$\overline{CS} \geq V_{IH}$ Address Change every t_{RC}	C		10		1.0	1.5	mA
			I		15			2.0	
			M		20			3.0	
Standby Supply Current with CMOS inputs	I_{FSB}	$\overline{CS} = V_{CC} \pm 0.2V$ No Address Transitions	C		2		0.025	0.75	mA
			I		5			1.25	
			M		10			2.5	
Data Retention Current	I_{CCDR2}	$\overline{CS} = V_{DR}$ min, V_{CC} = 2.0V	C		NA		5	100	µA
			I		NA			150	
			M		NA			600	
	I_{CCDR3}	$\overline{CS} = V_{DR}$ min, V_{CC} = 3.0V	C		NA		8	150	
			I		NA			225	
			M		NA			900	
Data Retention Voltage	V_{DR}	V_{CC} input voltage, minimum		NA		2.0			V
Output Low Voltage	V_{OL}	I_{OL} = 8 mA			0.4			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA		2.4		2.4			V

Pin Capacitance (Typical)	Test Conditions	Addresses	Data I/O	$\overline{CS}$, $\overline{WE}$, $\overline{OE}$	Units
	Pin Voltage = 0V, f=1.0 Mhz	8	10	12	pF

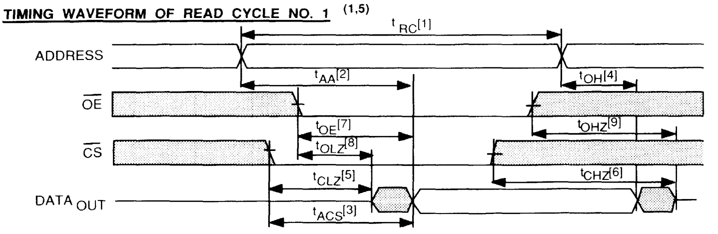
AC Characteristics (1)

No.	Parameter	Symbol	55 C,I		70 C,I,M		85 C,I,M		100 C,I,M		120 I,M	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
1	Read Cycle Time	t_{RC}	55		70		85		100		120	
2	Address Access Time	t_{AA}		55		70		85		100		120
3	$\overline{CS}$ Access Time	t_{ACS}		55		70		85		100		120
4	Output Hold from Address Change	t_{OH}	5		5		5		5		5	
5	$\overline{CS}$ Asserted to Output in Low Z	$t_{CLZ(2,3)}$	5		5		5		5		5	
6	$\overline{CS}$ Deasserted to Output in High Z	$t_{CHZ(2,3)}$	0	35	0	35	0	35	0	35	0	35
7	$\overline{OE}$ Asserted to Output Valid	t_{OE}		20		25		30		50		50
8	$\overline{OE}$ Asserted to Output in Low Z	$t_{OLZ(2,3)}$	0		0		0		0		0	
9	$\overline{OE}$ Asserted to Output in High Z	$t_{OHZ(2,3)}$	0	35	0	35	0	35	0	35	0	35
10	Write Cycle Time	t_{WC}	55		70		85		100		120	
11	Address Set-up Time	t_{AS}	0		0		0		0		0	
12	Write Pulse Width	t_{WP}	35		35		40		45		50	
13	Write Recovery Time	t_{WR}	5		5		5		5		5	
14	Data Hold Time	t_{DH}	3		3		3		3		3	
15	Data Valid to End of Write	t_{DW}	25		30		35		40		40	
16	Output Active from End of Write	$t_{WLZ(2,3)}$	5		5		5		5		5	
17	$\overline{WE}$ Asserted to Output in High Z	$t_{WHZ(2,3)}$	0	35	0	35	0	35	0	35	0	35
18	Chip Deselect to Data Retention Time	$t_{CDR(2)}$	0		0		0		0		0	
19	Operation Recovery Time	$t_{R(2)}$		55		70		85		100		120
20	$\overline{CS}$ Asserted to End of Write	t_{CW}	45		60		75		75		75	
21	Address Valid to End of Write	t_{AW}	45		60		75		75		75	

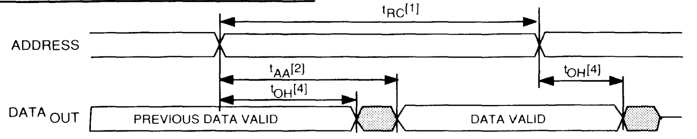
Notes: (1) At Recommended Operating Conditions. All Values in Nanoseconds. (2) This Parameter is characterized initially and after any design or process change which could affect it. It is guaranteed to, but not tested to, the limits specified. (3) All I/O Transitions are measured ± 500mV from steady state with loading as specified in "Load Test Circuits."

READ CYCLE

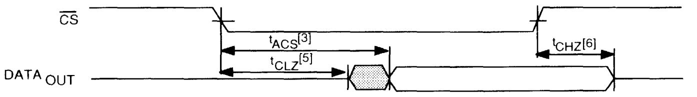
TIMING WAVEFORM OF READ CYCLE NO. 1 (1,5)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1,2,4,5)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1,2,3,5)



Reading the device is accomplished by taking chip select (CS) and output enable(OE) LOW, while write enable (WE) remains inactive or high. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

Notes:

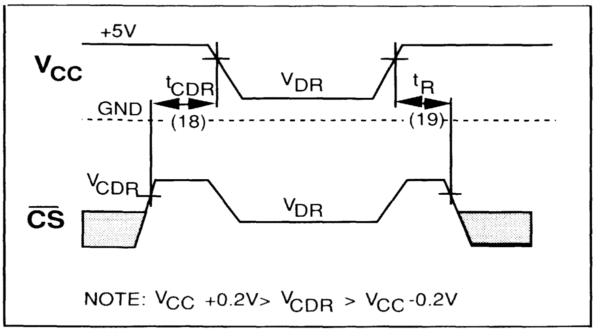
1. WE is high for READ CYCLES.
2. Device is continuously selected, CS= V_{IL} for all outputs active.
3. Address valid prior to or coincident with CS transition low.
4. OE =V_{IL}
5. Data Output transitions measured ± 500mV from steady state. This parameter is sampled and not 100% tested

Data Retention Cycle

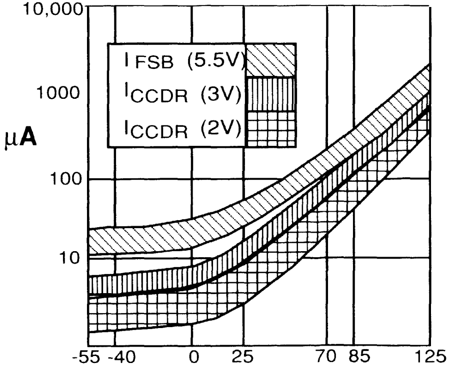
S32K8 devices exhibit very low current drain when operated in Data Retention Mode. This Mode is entered by first driving Chip Select to V_{CC} and subsequently driving both V_{CC} and Chip Select to V_{DR}. Chip Select must be set up before the V_{CC} drops below its minimum level. When exiting from Data Retention Mode, the user must wait one full Read Cycle Time prior to asserting Chip Select.

The curve showing typical device current is included to assist the user in understanding the relationship of the current required by the part when its Temperature and Voltage vary. The device is tested and guaranteed to conditions specified under DC and Operating Conditions.

DATA RETENTION MODE TIMING



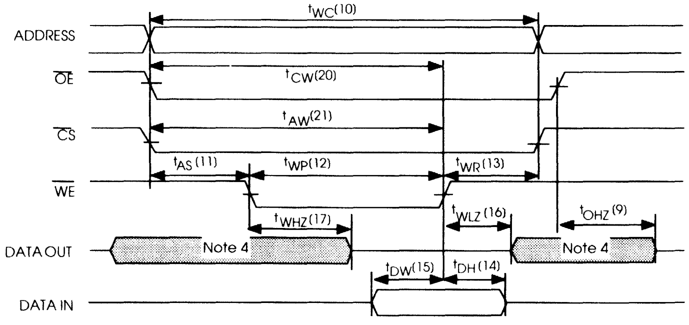
Standby Current, Typical



TEMPERATURE, DEG C

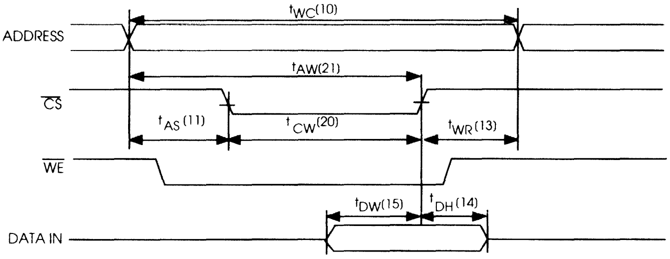
WRITE CYCLE

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING) (Notes 1,2,3,6,7)



(Notes 1,2,3,5,6)

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)



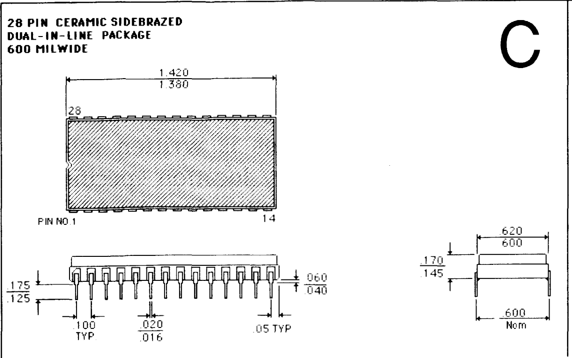
Writing to the S32K8 is achieved when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are LOW. Data on the input/output pins is written into the memory location specified on the address pins (A0-A14).

The input/output pins remain in a high impedance state when chip select ($\overline{CS}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

Notes:

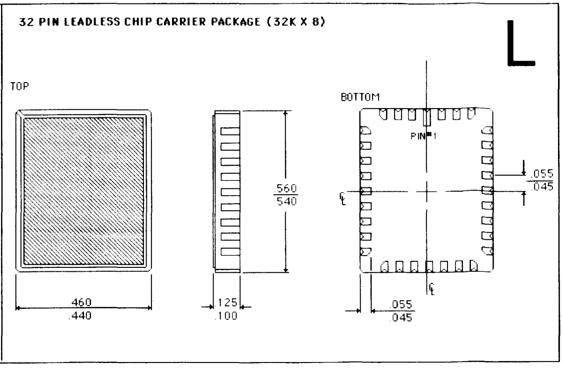
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transitions occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Data output transitions are measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse low is $\geq t_{DW} + t_{WHZ}$ to allow the I/O drivers to turn off and data to be placed on the the bus for the required TDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified TWP.

Package Dimension and Ordering Information



28 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
600 MILWIDE

C



32 PIN LEADLESS CHIP CARRIER PACKAGE (32K X 8)

L

S32K8X-45XX

X
C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (-40°C to 85°C)
M = Military Temperature Range (-55°C to 125°C)

C = 600 mil Ceramic Sidebrazed DIP
L = Leadless Chip Carrier

L suffix on base part number = Low Power Device

Printed in U.S.A., AMN-790

128K x 8 Static RAM

Key Parameters S128K8 and S128K8L	Device Types							
	25C	35M 35I 35C	45M 45I 45C	55M 55I 55C	70M 70I 70C	85M 85I 85C	100M 100I 100C	Unit
Access Time	25	35	45	55	70	85	100	nS
Cycle Time	25	35	45	55	70	85	100	nS
Output Enable Access	10	15	15	20	25	30	50	nS

Features

- **32 pin DIP, LCC, SOJ, Flatpack**
- **Advanced 4-T CMOS technology**
- **S128K8 is compliant to DESC Standardized Military Drawing No. 5962-89598**
- **300 mil DIP for 25, 35, 45 ns parts**
- **Military, industrial, and commercial temperature range**
- **Military grades compliant to MIL-STD-883C**

General Description

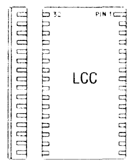
The Inova S128K8 is a high performance one megabit Static Random Access Memory (SRAM) organized as 128K eight -bit bytes.

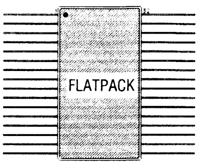
The S128K8 is manufactured using a highly reliable, four transistor cell CMOS process. This provides a component which combines low active and standby power characteristics with high performance.

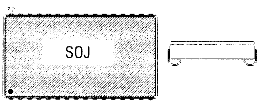
All inputs are fully TTL-compatible. Operation is fully static, without need for extra control logic to generate clock signals.

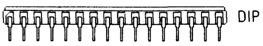
Every military grade device is fully compliant to MIL-STD-883C, paragraph 1.2.1. Industrial and commercial grade devices are fabricated in the same production line which assures that they are also of the highest quality.

Package Options









Pinout

1	NC	32	VCC
2	A16	31	A15
3	A14	30	NC
4	A12	29	$\overline{WE}$
5	A7	28	A13
6	A6	27	A8
7	A5	26	A9
8	A4	25	A11
9	A3	24	$\overline{OE}$
10	A2	23	A10
11	A1	22	$\overline{CS}$
12	A0	21	I/O7
13	I/O0	20	I/O6
14	I/O1	19	I/O5
15	I/O2	18	I/O4
16	VSS	17	I/O3

A0-A16	Address Inputs
I/O0-I/O7	Data Input/ Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
VCC	+5V Power
VSS	Ground

Recommended Operating Conditions

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*
Supply Voltage(1)	V_{CC}	4.5	5.5	V
Input HIGH Voltage	V_{IH}	2.2	V_{CC}+0.5	V
Input LOW Voltage	V_{IL}	-0.5	0.8	V
Operating Temp. Mil.	T_C	-55	125	°C
Operating Temp. Ind.	T_C	-40	85	°C
Operating Temp. Comm.	T_C	0	70	°C

Absolute Maximum Ratings (2)

Temperature Under Bias	-55 °C to 125 °C
Storage Temperature	-65 °C to 150 °C
Supply Voltage(1)	-0.5V to 7.0 V
Signal Voltage On Any Pin	-0.5 V to V_{CC} + 0.5V
Power Dissipation	1 Watt
D.C. Continuous Output Current Per Output	20 mA
Lead Temperature (Soldering 10 sec)	260 °C

Notes:

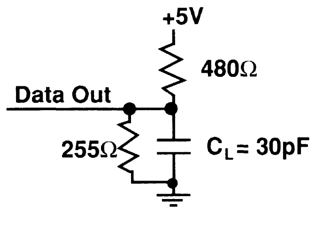
1. All voltages referenced to V_{SS} (GND).

2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	*I/O Operation*	*Supply Current*
Standby	H	X	X	High Z	I_{SB}/I_{FSB}
Read	L	L	H	Output	I_{CC2}
Write	L	X	L	Input	I_{CC2}
Output Disable	L	H	H	High Z	I_{CC2}

Load Test Circuits



C_L = 5pF for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{WLZ}.

Memory Scale

Access Time	25	35	45	55	70	85	100	**Unit**
S128K8	40	29	22	18	14	11	10	kbits/ns

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

DC and Operating Characteristics L=Low Power, S = Standard Power

Symbol		25		35		45		55		70		85		100		Units
		L	S	L	S	L	S	L	S	L	S	L	S	L	S	
I_{CC1} (1)	C	90	100	80	90	80	90	80	90	80	90	80	90	80	90	mA(max)
	I	----	----	85	95	85	95	85	95	85	95	85	95	85	95	
	M	----	----	90	100	90	100	90	100	90	100	90	100	90	100	
I_{CC2} (2)		140	150	125	140	125	125	125	125	125	125	125	125	125	125	mA(max)
I_{SB} (3)	C	30	40	3	30	1.5	4	1.5	4	1.5	4	1.5	4	1.5	4	mA(max)
	I	----	----	4	35	2.0	5	2.0	5	2.0	5	2.0	5	2.0	5	
	M	----	----	10	40	10	10	10	10	10	10	10	10	10	10	
I_{FSB} (4)	C	0.75	----	0.75	----	0.75	----	0.75	----	0.75	----	0.75	----	0.75	----	mA(max)
	I	----	----	1.25	----	1.25	----	1.25	----	1.25	----	1.25	----	1.25	----	
	M	----	----	5	----	5	----	5	----	5	----	5	----	5	----	
I_{CCDR} (5)	C	0.10	----	0.10	----	0.10	----	0.10	----	0.10	----	0.10	----	0.10	----	mA(max)
	I	----	----	0.15	----	0.15	----	0.15	----	0.15	----	0.15	----	0.15	----	
	M	----	----	2.0	----	2.0	----	2.0	----	2.0	----	2.0	----	2.0	----	
V_{DR} (6)		2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	V(min)

Notes:

(1) Static Supply Current: $\overline{CS}=V_{IL}$, $\overline{OE}=V_{IH}$, No address transitions

(2) Dynamic Supply Current: $\overline{CS} < V_{IL}$, $\overline{OE}=V_{IH}$, Address Change every t_{RC}

(3) Standby Supply Current With TTL Inputs:
$\overline{CS} > V_{IH}$, Address change every t_{RC}

(4) Standby Supply Current With CMOS Inputs: $\overline{CS} = V_{CC}+0.2V$, No address transitions

(5) Data Retention Current: $\overline{CS} = V_{DR}$ min, $V_{CC} = V_{DR}$ min

(6) Data Retention Voltage: V_{CC} minimum supply voltage

DC and Operating Characteristics L=Low Power, S = Standard Power

Symbol	25		35		45		55		70		85		100		Units
	L	S	L	S	L	S	L	S	L	S	L	S	L	S	
$\lvert I_{LI} \rvert$ (1)	2	2	2	2	2	2	2	2	2	2	2	2	2	2	µA(max)
$\lvert I_{LO} \rvert$ (2)	2	2	2	2	2	2	2	2	2	2	2	2	2	2	µA(max)
V_{OL} (3)	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	V (max)
V_{OH} (4)	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	V (min)

Typical Pin Capacitance	*Test Conditions*	*Addresses*	*Data I/O*	*$\overline{CS}$, $\overline{WE}$, $\overline{OE}$*	
	Pin Voltage=0V, *f*=1.0 MHz	8	10	12	pF(typ)

Notes:

(1) Input Leakage Current: V_{CC} = max, V_{IN} = GND to V_{CC}

(2) Output Leakage Current: V_{OUT} = GND to V_{CC}, Outputs in tri-state

(3) Output Low Voltage: I_{OL} = 8 mA

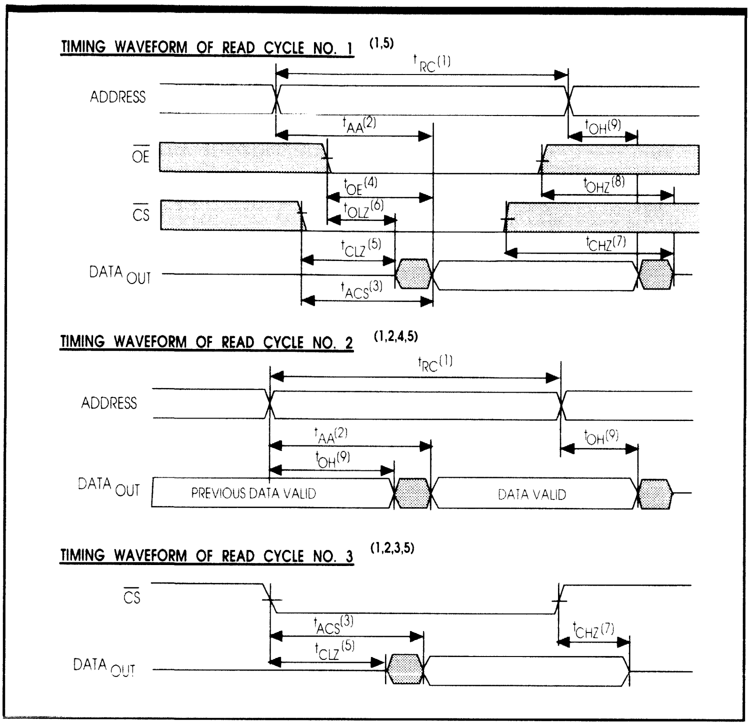
(4) Output High Voltage: I_{OH} = -4 mA

AC Characteristics(1)

No.	S128K8 and S128K8L Parameter	Symbol	25C		35C,I,M		45C,I,M		55C,I,M		70 C,I,M		85C,I,M	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min
1	Read Cycle Time	t_{RC}	25		35		45		55		70		85	
2	Address Access Time	t_{AA}		25		35		45		55		70		85
3	$\overline{CS}$ on to Output Valid	t_{ACS}		25		35		45		55		70		85
4	$\overline{OE}$ on to Output Valid	t_{OE}		10		15		15		20		25		30
5	$\overline{CS}$ on to Output in Low Z	$t_{CLZ}^{(2,3)}$	5		5		5		5		5		5	
6	$\overline{OE}$ on to Output in Low Z	$t_{OLZ}^{(2,3)}$	0		0		0		0		0		0	
7	$\overline{CS}$ off to Output in High Z	$t_{CHZ}^{(2,3)}$	0	10	0	15	0	20	0	35	0	35	0	35
8	$\overline{OE}$ off to Output in High Z	$t_{OHZ}^{(2,3)}$	0	10	0	15	0	20	0	35	0	35	0	35
9	Output Hold from Address Change	t_{OH}	3		5		5		5		5		5	
10	Write Cycle Time	t_{WC}	25		35		45		55		70		85	
11	Chip Selection to End of Write	t_{CW}	20		25		35		45		60		75	
12	Address Set-up Time	t_{AS}	0		0		0		0		0		0	
13	Address Valid to End of Write	t_{AW}	20		25		35		45		60		75	
14	Write Pulse Width	t_{WP}	20		25		30		35		35		40	
15	Write Recovery Time	t_{WR}	0		0		5		5		5		5	
16	Write Pulse on to Output in High Z	$t_{WHZ(2,3)}$	0	10	0	15	0	20	0	35	0	35	0	35
17	Write Pulse off to Output in Low Z	$t_{WLZ(2,3)}$	5		5		5		5		5		5	
18	Data Valid Set-Up to End of Write	t_{DW}	15		20		25		25		30		35	
19	Data Hold from End of Write	t_{DH}	0		0		0		3		3		3	
20	Chip Deselect to Data Retention	$t_{CDR(2)}$	0		0		0		0		0		0	
21	Operation Recovery Time	$t_{R(2)}$		25		35		45		55		70		85

Notes: (1) At Recommended Operating Conditions. All Values in Nanoseconds. 100nS and 120nS parts are also available. (2) This Parameter is characterized initially and after any design or process change which could affect it. It is guaranteed to, but not tested to, the limits specified. (3) All Transitions are measured ± 500mV from steady state with loading as specified in "Load Test Circuits."

READ CYCLE



Reading the S128K8 device is accomplished by taking chip select ($\overline{CS}$) and output enable($\overline{OE}$) LOW , while write enable ($\overline{WE}$) remains inactive or high. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

Notes:

1. $\overline{WE}$ is high for READ CYCLES.

2. Device is continuously selected, $\overline{CS}$= V_{IL} for all outputs active.

3. Address valid prior to or coincident with $\overline{CS}$ transition low.

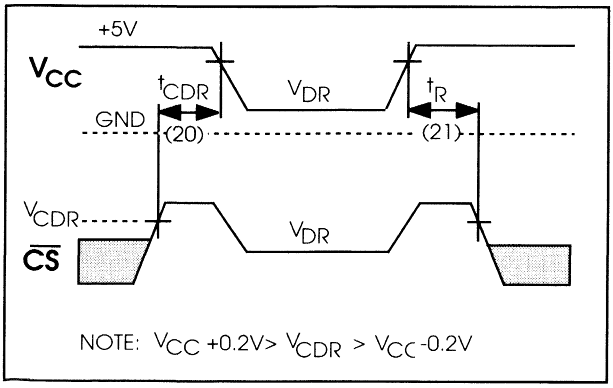
4. $\overline{OE}$ =V_{IL}

5. Data Output transitions measured ±500mV from steady state. This parameter is sampled and not 100% tested

Data Retention

S128K8 devices exhibit very low current drain when operated in Data Retention Mode. This Mode is entered by first driving Chip Select to V_{CC} and subsequently driving both V_{CC} and Chip Select to V_{DR}. Chip Select must be set up before the V_{CC} drops below its minimum level. When exiting from Data Retention Mode, the user must wait one full Read Cycle Time prior to asserting Chip Select.

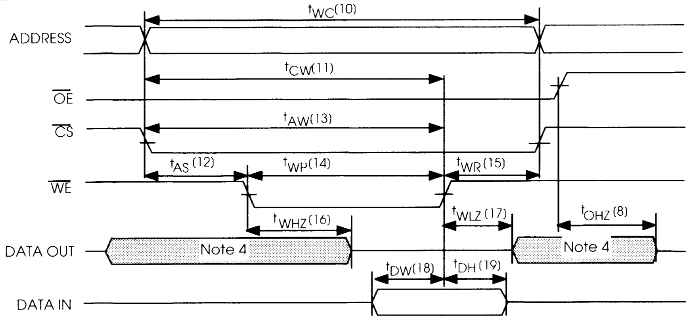
DATA RETENTION TIMING



NOTE: V_{CC} +0.2V> V_{CDR} > V_{CC}-0.2V

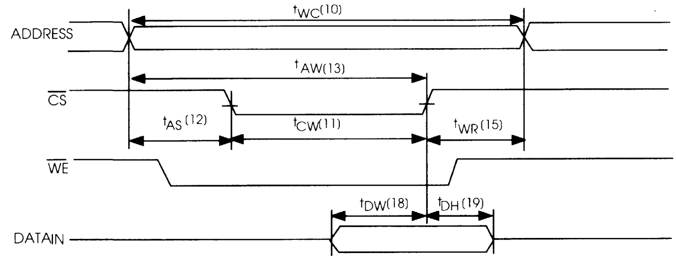
WRITE CYCLE

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{\text{WE}}$ CONTROLLED TIMING) (Notes 1,2,3,6,7)



(Notes 1,2,3,5,6)

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ CONTROLLED TIMING)



Writing to the S128K8 is achieved when the chip select (CS) and write enable (WE) inputs are LOW. Data on the input/output pins is written into the memory location specified on the address pins (A0-A16).

The input/output pins remain in a high impedance state when chip select (CS) or output enable (OE) is HIGH, or write enable (WE) is LOW.

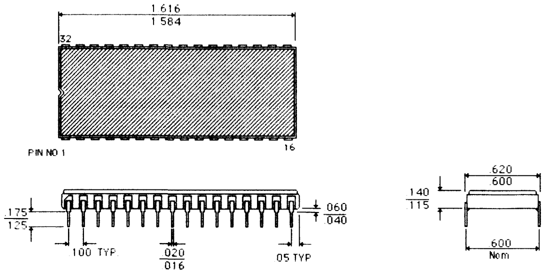
Notes:

1. $\overline{\text{WE}}$ or $\overline{\text{CS}}$ must be high during all address transitions.
2. A write occurs during the overlap (TWP) of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$.
3. TWR is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{\text{CS}}$ low transitions occurs simultaneously with or after the $\overline{\text{WE}}$ low transition, the outputs remain in a high impedance state.
6. Data output transitions are measured $\pm$ 500mV from steady state. This parameter is sampled and characterized but not 100% tested.
7. During a $\overline{\text{WE}}$ controlled write cycle, write pulse low is $\geq$TDW + TWHZ to allow the I/O drivers to turn off and data to be placed on the the bus for the required TDW. If $\overline{\text{OE}}$ is high during a WE controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified TWP.

Package Dimension and Ordering Information

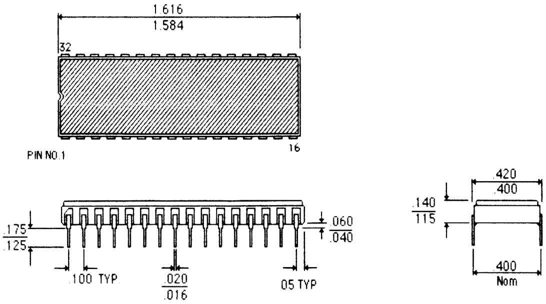
**32 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
600 MIL WIDE**

C



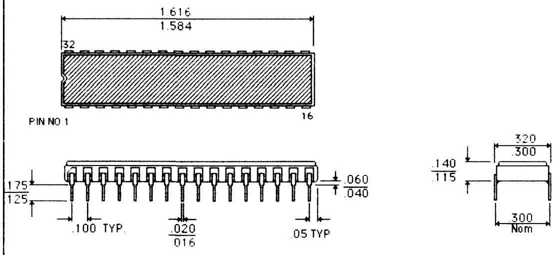
**32 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
400 MIL WIDE**

E

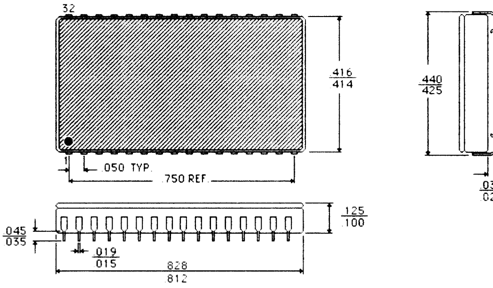


**32 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
300 MIL WIDE**

T

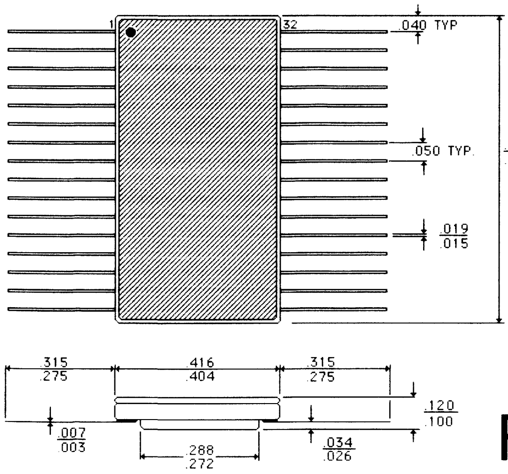


32 PIN CERAMIC "J" LEADED 400 MIL WIDE PACKAGE



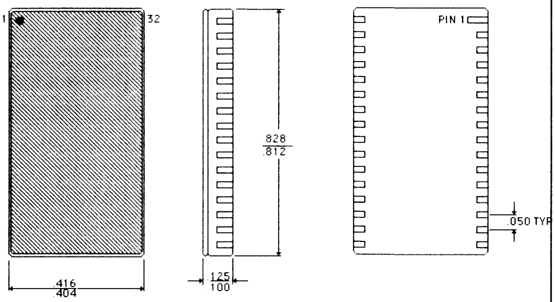
S

32 PIN CERAMIC FLATPACK, 400 MIL WIDE PACKAGE



F

32 PIN LEADLESS CHIP CARRIER PACKAGE

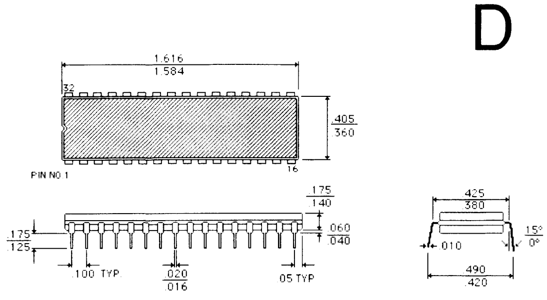


L

Package Dimension and Ordering Information

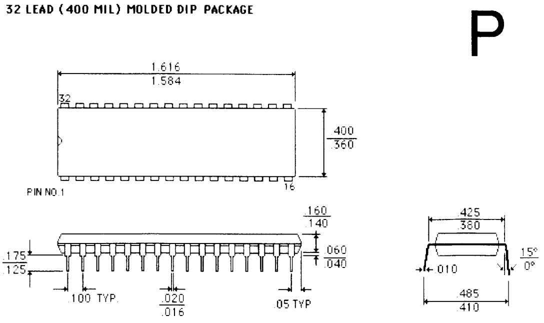
32 LEAD (400 MIL) CERDIP PACKAGE

D



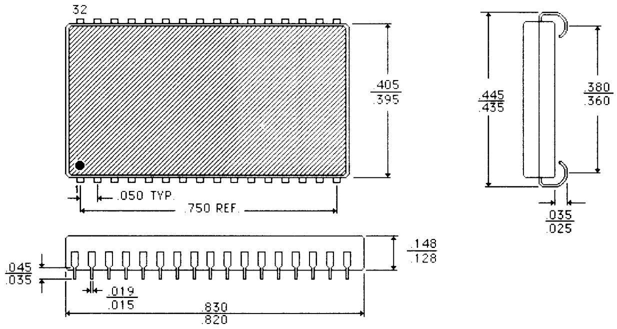
32 LEAD (400 MIL) MOLDED DIP PACKAGE

P



32 PIN PLASTIC SOJ PACKAGE,400 MIL WIDE BODY

J



S128K8X-45XX

C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (-40°C to 85°C)
M = Military Temperature Range (-55°C to 125°C)

C = 600 mil Ceramic Sidebrazed DIP
D = 400 mil CERDIP
E = 400 mil Ceramic Sidebrazed DIP
T = 300 mil Ceramic Sidebrazed DIP
P = 400 mil Plastic DIP
F = Flatpack
S = Ceramic SOJ
J = Plastic SOJ
L = Leadless Chip Carrier

L suffix on base part number = Low Power Device

All Specifications are subject to change without notice.
Printed in U.S.A., AMN-790

inova microelectronics

S128K8T

Product Data

128K x 8 Static RAM

Key Parameters	***Device Types***							
S128K8T and S128K8TL	***25C***	***35M 35I 35C***	***45M 45I 45C***	***55M 55I 55C***	***70M 70 70C***	***85M 85I 85C***	***100M 100I 100C***	***Unit***
Access Time	25	35	45	55	70	85	100	nS
Cycle Time	25	35	45	55	70	85	100	nS
Output Enable Access	10	15	15	20	25	30	50	nS

Features

- **Two Chip Selects for Increased Flexibility**
- **Fully static 128Kx8 SRAM**
- **Advanced 4-T CMOS technology**
- **32 pin DIP, LCC, SOJ, and Flatpack**
- **300 mil DIP for 25, 35, 45 ns parts**
- **Military, industrial, and commercial temperature range**
- **Military grades compliant to MIL-STD-883C**

General Description

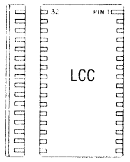
The Inova S128K8T is a high performance one megabit Static Random Access Memory (SRAM) organized as 128K eight -bit bytes.

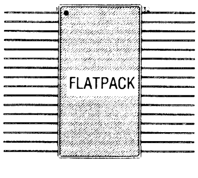
The S128K8T is manufactured using a highly reliable, four transistor cell CMOS process. This provides a component which combines low active and standby power characteristics with high performance.

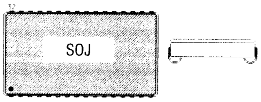
All inputs are fully TTL-compatible. Operation is fully static, without need for extra control logic to generate clock signals.

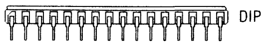
Every military grade device is fully compliant to MIL-STD-883C, paragraph 1.2.1. Industrial and commercial grade devices are fabricated in the same production line which assures that they are also of the highest quality.

Package Options









Pinout

1	**NC**	32	**VCC**
2	**A16**	31	**A15**
3	**A14**	30	**CS2**
4	**A12**	29	**$\overline{WE}$**
5	**A7**	28	**A13**
6	**A6**	27	**A8**
7	**A5**	26	**A9**
8	**A4**	25	**A11**
9	**A3**	24	**$\overline{OE}$**
10	**A2**	23	**A10**
11	**A1**	22	**$\overline{CS1}$**
12	**A0**	21	**I/O7**
13	**I/O0**	20	**I/O6**
14	**I/O1**	19	**I/O5**
15	**I/O2**	18	**I/O4**
16	**VSS**	17	**I/O3**

A0-A16	Address Inputs
I/O0-I/O7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS1}$	Chip Select 1
CS2	Chip Select 2
VCC	+5V Power
VSS	Ground

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage(1)	V_{CC}	4.5	5.5	V
Input HIGH Voltage	V_{IH}	2.2	V_{CC}+0.5	V
Input LOW Voltage	V_{IL}	-0.5	0.8	V
Operating Temp. Mil.	T_C	-55	125	°C
Operating Temp. Ind.	T_C	-40	85	°C
Operating Temp. Comm.	T_C	0	70	°C

Absolute Maximum Ratings (2)

Temperature Under Bias	-55 °C to 125 °C
Storage Temperature	-65 °C to 150 °C
Supply Voltage(1)	-0.5V to 7.0 V
Signal Voltage On Any Pin	-0.5 V to V_{CC} + 0.5V
Power Dissipation	1 Watt
D.C. Continuous Output Current Per Output	20 mA
Lead Temperature (Soldering 10 sec)	260 °C

Notes:

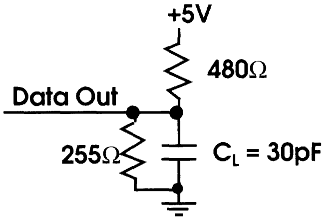
1. All voltages referenced to V_{SS} (GND).

2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Truth Table

Mode	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	X	High Z	I_{SB}/I_{FSB}
Standby	X	L	X	X	High Z	I_{SB}/I_{FSB}
Read	L	H	L	H	Output	I_{CC2}
Write	L	H	X	L	Input	I_{CC2}
Output Disable	L	H	H	H	High Z	I_{CC2}

Load Test Circuits



C_L = 5pF for $t_{CLZ1,2}$, $t_{CHZ1,2}$, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{WLZ}.

Memory Scale

Access Time	25	35	45	55	70	85	100	Unit
S128K8	40	29	22	18	14	11	10	kbits/ns

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

DC and Operating Characteristics

L = Low Power, S = Standard Power

Symbol		25		35		45		55		70		85		100		Units
		L	S	L	S	L	S	L	S	L	S	L	S	L	S	
I_{CC1} (1)	C	90	100	80	90	80	90	80	90	80	90	80	90	80	90	mA(max)
	I	----	----	85	95	85	95	85	95	85	95	85	95	85	95	
	M	----	----	90	100	90	100	90	100	90	100	90	100	90	100	
I_{CC2} (2)		150	140	125	140	125	125	125	125	125	125	125	125	125	125	mA(max)
I_{SB} (3)	C	30	40	3	30	3	5	3	5	3	5	3	5	3	5	mA(max)
	I	----	----	4	35	4	6	4	6	4	6	4	6	4	6	
	M	----	----	10	40	10	10	10	10	10	10	10	10	10	10	
I_{FSB} (4)	C	0.75	----	0.75	----	0.75	----	0.75	----	0.75	----	0.75	----	0.75	----	mA(max)
	I	----	----	1.25	----	1.25	----	1.25	----	1.25	----	1.25	----	1.25	----	
	M	----	----	5	----	5	-----	5	----	5	----	5	----	5	----	
I_{CCDR} (5)	C	0.10	----	0.10	----	0.10	----	0.10	----	0.10	----	0.10	----	0.10	----	mA(max)
	I	----	----	0.15	----	0.15	----	0.15	----	0.15	----	0.15	----	0.15	----	
	M	----	----	2	----	2.0	----	2.0	----	2.0	----	2.0	----	2.0	----	
V_{DR} (6)		2.0	2.0	2.0	2.0	2.0	2.0	2.0	----	2.0	----	2.0	----	2.0	----	V (min)

Notes:

(1) Static Supply Current: $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, $\overline{OE}$ = V_{IH}, No address transitions

(2) Dynamic Supply Current: $\overline{CS1} \leq V_{IL}$, CS2 $\geq V_{IH}$, $\overline{OE}$= V_{IH}, Address Change every t_{RC}

(3) Standby Supply Current (TTL): $\overline{CS1} > V_{IH}$, CS2 < V_{IL}, Address change every t_{RC}

(4) Standby Supply Current (CMOS): $\overline{CS1}$ = V_{CC}±0.2V or CS2 ≤ 0.2V, No address transitions

(5) Data Retention Current: $\overline{CS1}$ = V_{DR} min, CS2 ≤ 0.2V, V_{CC} = V_{DR} min

(6) Data Retention Voltaget: V_{CC} minimum supply voltage

DC and Operating Characteristics

L=Low Power, S = Standard Power

Symbol	25		35		45		55		70		85		100		Units
	L	S	L	S	L	S	L	S	L	S	L	S	L	S	
$\lvert I_{LI} \rvert$ (1)	2	2	2	2	2	2	2	2	2	2	2	2	2	2	µA(max)
$\lvert I_{LO} \rvert$ (2)	2	2	2	2	2	2	2	2	2	2	2	2	2	2	µA(max)
V_{OL} (3)	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	V (max)
V_{OH} (4)	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	V (min)

Typical Pin Capacitance	*Test Conditions*	*Addresses*	*Data I/O*	*$\overline{CS1}$, CS2, $\overline{WE}$, $\overline{OE}$*	
	Pin Voltage=0V, *f*=1.0 MHz	8	10	12	pF(typ)

Notes:

(1) Input Leakage Current: V_{CC} = max, V_{IN} = GND to V_{CC}, I_{LI} = 5µA for CS2 only

(2) Output Leakage Current: V_{OUT} = GND to V_{CC}, CS1 > V_{IH} or CS2 < V_{IL}

(3) Output Low Voltage: I_{OL} = 8 mA

(4) Output High Voltage: I_{OH} = -4 mA

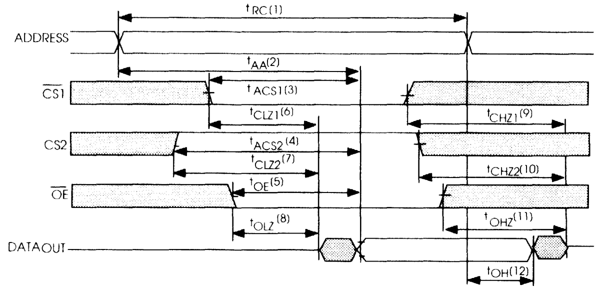
AC Characteristics(1)

No.	S128K8 and S128K8L Parameter	Symbol	25C		35C,I,M		45C,I,M		55C,I,M		70 C,I,M		85C,I,M	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
1	Read Cycle Time	t_{RC}	25		35		45		55		70		85	
2	Address Access Time	t_{AA}		25		35		45		55		70		85
3	$\overline{CS}$1 on to Output Valid	t_{ACS1}		25		35		45		55		70		85
4	CS2 on to Output Valid	t_{ACS2}		25		35		45		55		70		85
5	$\overline{OE}$ on to Output Valid	t_{OE}		10		15		15		20		25		30
6	$\overline{CS}$1 on to Output in Low Z	t_{CLZ1}(2,3)	5		5		5		5		5		5	
7	CS2 on to Output in Low Z	t_{CLZ2}(2,3)	5		5		5		5		5		5	
8	$\overline{OE}$ on to Output in Low Z	t_{OLZ}(2,3)	0		0		0		0		0		0	
9	$\overline{CS}$1 off to Output in High Z	t_{CHZ1}(2,3)	0	10	0	15	0	20	0	35	0	35	0	35
10	CS2 off to Output in High Z	t_{CHZ2}(2,3)	0	10	0	15	0	20	0	35	0	35	0	35
11	$\overline{OE}$ off to Output in High Z	t_{OHZ}(2,3)	0	10	0	15	0	20	0	35	0	35	0	35
12	Output Hold from Address Change	t_{OH}	3		5		5		5		5		5	
13	Write Cycle Time	t_{WC}	25		35		45		55		70		85	
14	Chip Selection to End of Write	t_{CW}	20		30		35		45		60		75	
15	Address Set-up Time	t_{AS}	0		0		0		0		0		0	
16	Address Valid to End of Write	t_{AW}	20		30		35		45		60		75	
17	Write Pulse Width	t_{WP}	20		25		30		35		35		40	
18	Write Recovery Time	t_{WR}	0		0		5		5		5		5	
19	Write Pulse on to Output in High Z	$t_{WHZ(2,3)}$	0	10	0	15	0	20	0	35	0	35	0	35
20	Write Pulse off to Output in Low Z	$t_{WLZ(2,3)}$	5		5		5		5		5		5	
21	Data Valid Set-Up to End of Write	t_{DW}	15		20		25		25		30		35	
22	Data Hold from End of Write	t_{DH}	0		0		0		3		3		3	
23	Chip Deselect to Data Retention	$t_{CDR(2)}$	0		0		0		0		0		0	
24	Operation Recovery Time	$t_{R(2)}$		25		35		45		55		70		85

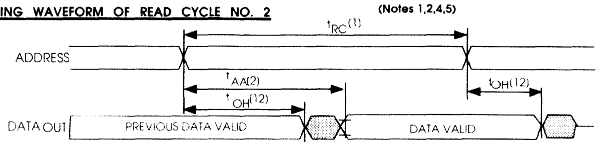
Notes: (1) At Recommended Operating Conditions. All Values in Nanoseconds. 100nS and 120nS parts are also available. (2) This Parameter is characterized initially and after any design or process change which could affect it. It is guaranteed to, but not tested to, the limits specified. (3) All Transitions are measured ± 500mV from steady state with loading as specified in "Load Test Circuits."

READ CYCLE

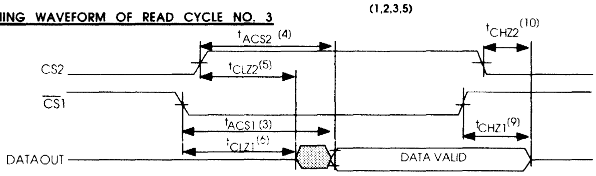
TIMING WAVEFORM OF READ CYCLE NO. 1 (Notes 1,5)



TIMING WAVEFORM OF READ CYCLE NO. 2 (Notes 1,2,4,5)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1,2,3,5)



Reading the S128KT device is accomplished by taking CS2 high and $\overline{\text{CS1}}$ and $\overline{\text{OE}}$ low, while $\overline{\text{WE}}$ remains inactive or high.

Under these conditions, the contents of the memory location specified on the adress pins will appear on the appropriate data/output pins.

Notes:

1. $\overline{\text{WE}}$ is above V_{IH} min for READ CYCLES.

2. Device is continuously selected, $\overline{\text{CS1}}=V_{IL}$, CS2=V_{IH} for all outputs active.

3. Address Valid prior to or coincident with CS transitions.

4. $\overline{\text{OE}} = V_{IL}$

5. Data Output transitions measured ±500mV from steady state. This parameter is sampled and not 100% tested.

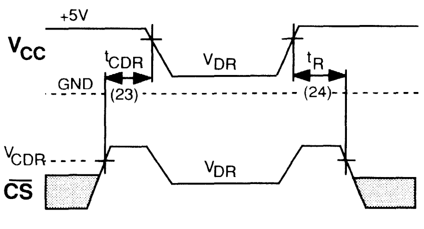
Data Retention

S128K8T devices exhibit very low current drain when operated in Data Retention mode. This mode is entered by either:

A) $\overline{\text{CS1}}$ controlled: Driving $\overline{\text{CS1}} \geq V_{CC}$ - 0.2V (0V≤ CS2 to ≤0.2V) and subsequently driving both V_{CC} and $\overline{\text{CS1}}$ to V_{DR}.

B) CS2 controlled: Driving CS2 to 0V≤CS2≤0.2V, and subsequently driving V_{cc} to V_{DR}. When exiting from Data Retention mode, the user must wait one full Read Cycle Time prior to asserting either $\overline{\text{CS1}}$ or CS2.

DATA RETENTION TIMING



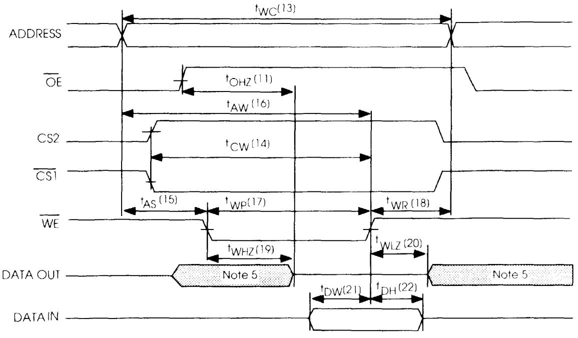
NOTE: V_{CC} +0.2V> V_{CDR} > V_{CC} -0.2V

WRITE CYCLE

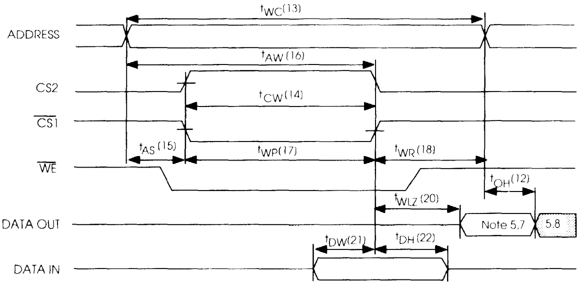
Writing to the S128K8T is achieved when the chip select CS2 is high and $\overline{\text{CS1}}$ and $\overline{\text{WE}}$ inputs are LOW. Data on the input/output pins is written into the memory location specified on the address pins (A0-A16).

The input/output pins remain in a high impedance state when CS2 or $\overline{\text{WE}}$ is LOW, or $\overline{\text{CS1}}$ or $\overline{\text{OE}}$ is HIGH.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{\text{OE}}$ CLOCKED)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{OE}}$ HELD LOW)



NOTES

1. A Write occurs during the overlap of a low $\overline{\text{CS1}}$, a high CS2 and a low $\overline{\text{WE}}$. A Write begins at the latest transition among $\overline{\text{CS1}}$ going low, CS2 going high and $\overline{\text{WE}}$ going low. A Write ends at the earliest transition among $\overline{\text{CS1}}$ going high, CS2 going low and $\overline{\text{WE}}$ going high. During a $\overline{\text{WE}}$ controlled write cycle, write pulse low is ≥TDW + TWHZ to allow the I/O drivers to turn off and data to be placed on the bus for the required TDW. If $\overline{\text{OE}}$ is high during a $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified TWP.

2. TCW is measured from the later of $\overline{\text{CS1}}$ going low or CS2 going high to the end of write.

3. TAS is measured from the address valid to the beginning of write.

4. TWR is measured from the earliest of $\overline{\text{CS1}}$ or $\overline{\text{WE}}$ going high or CS2 going low to the end of write.

5. During this period, I/O pins are in the output state, therefore input signals of opposite phase must not be applied.

6. If $\overline{\text{CS1}}$ goes low and CS2 goes high simultaneously with $\overline{\text{WE}}$ going low or after $\overline{\text{WE}}$ goes low, the outputs remain in a high impedance state.

7. DATA OUT is the same data written during the present cycle.

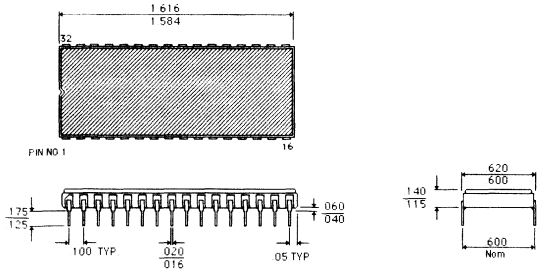
8. The real data of the next address is present at DATA OUT TAA after the address transition.

9. The tri-state parameters of data input and output are sampled and characterized, but not 100% tested.

Package Dimension and Ordering Information

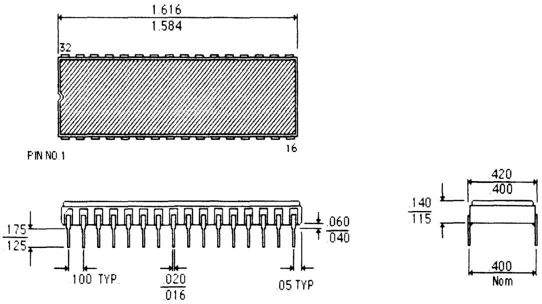
32 PIN CERAMIC SIDEBRAZED DUAL-IN-LINE PACKAGE 600 MIL WIDE

C



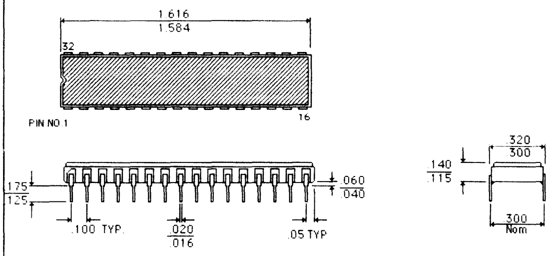
32 PIN CERAMIC SIDEBRAZED DUAL-IN-LINE PACKAGE 400 MIL WIDE

E

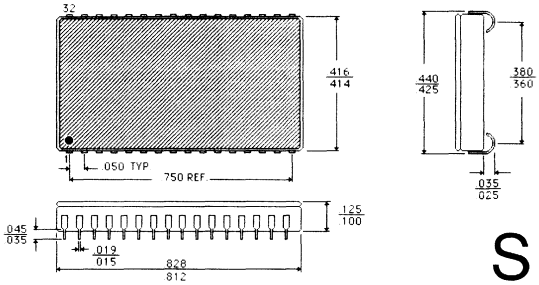


32 PIN CERAMIC SIDEBRAZED DUAL-IN-LINE PACKAGE 300 MIL WIDE

T

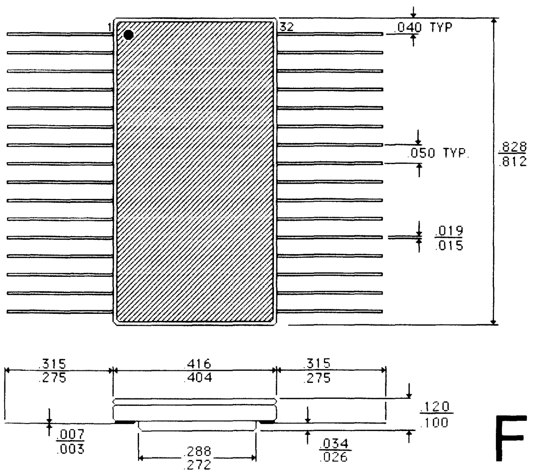


32 PIN CERAMIC "J" LEADED 400 MIL WIDE PACKAGE



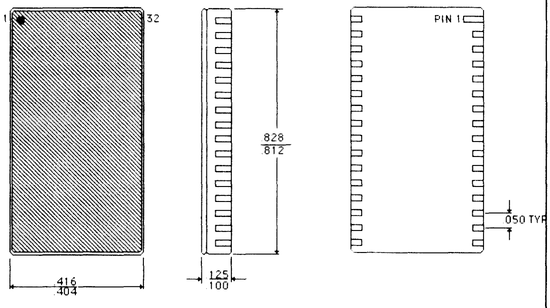
S

32 PIN CERAMIC FLATPACK,400 MIL WIDE PACKAGE



F

32 PIN LEADLESS CHIP CARRIER PACKAGE

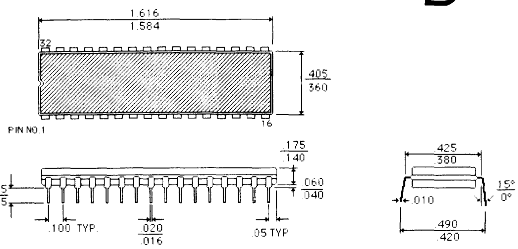


L

Package Dimension and Ordering Information

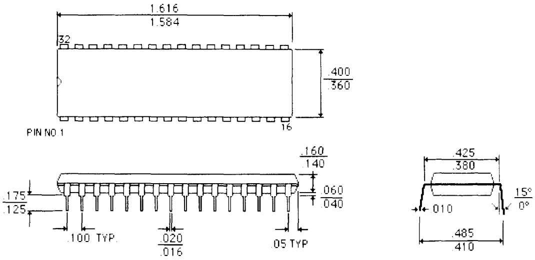
32 LEAD (400 MIL) CERDIP PACKAGE

D



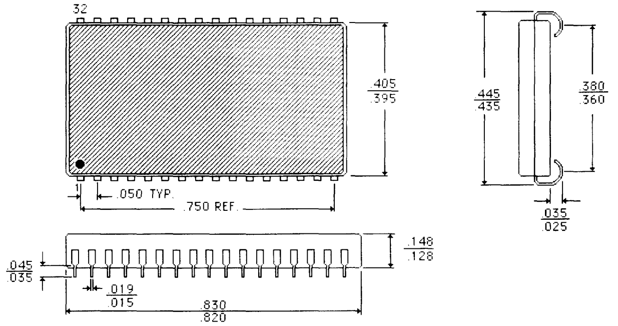
32 LEAD (400 MIL) MOLDED DIP PACKAGE

P



32 PIN PLASTIC SOJ PACKAGE, 400 MIL WIDE BODY

J



S128K8TX-45XX

C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (-40°C to 85°C)
M = Military Temperature Range (-55°C to 125°C)

C = 600 mil Ceramic Sidebrazed DIP
D = 400 mil CERDIP
E = 400 mil Ceramic Sidebrazed DIP
T = 300 mil Ceramic Sidebrazed DIP
P = 400 mil Plastic DIP
F = Flatpack
S = Ceramic SOJ
J = Plastic SOJ
L = Leadless Chip Carrier

L suffix on base part number = Low Power Device

All Specifications are subject to change without notice.
Printed in U.S.A., AMN-790

inova microelectronics **S64K16**

Product Data

64K x 16 Static RAM

Key Parameters S64K16 and S64K16L	Device Types						
	45CC	55MC 55 IC 55 CC	70 MC 70 IC 70 CC	85 MC 85 IC 85 CC	100 MC 100 IC 100 CC	120 MC 120 IC	Unit
Access Time	45	55	70	85	100	120	nS
Cycle Time	45	55	70	85	100	120	nS
Output Enable Access	20	20	25	30	50	50	nS

Features

- **Monolithic 64K x 16 SRAM**
- **Advanced 4-T CMOS technology**
- **40 pin JEDEC standard pinout**
- **S64K16 is compliant to DESC Standardized Military Drawing No. 5962-90858**
- **Military, industrial, and commercial temperature range**
- **Military grade compliant to MIL-STD-883C**
- **2.0V Low-Power Data Retention Option (S64K16L)**

General Description

The Inova S64K16 is a high performance one megabit Static Random Access Memory (SRAM), organized as 64K sixteen-bit bytes.

The S64K16 is manufactured using a highly reliable, four transistor cell CMOS process. This provides a component which combines low active and standby power characteristics with high performance.

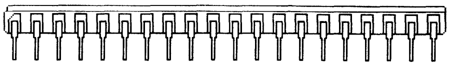
All inputs and outputs are fully TTL compatible. Operation is fully static, so there is no need for extra control logic to generate clocks and timing strobes.

Every military grade device is fully compliant to MIL-STD-883C, paragraph 1.2.1. Industrial and commercial grade devices are produced in the same production line which ensures that they are also of the highest quality.

Pinout/Package Options

1	A15	40	VCC
2	$\overline{\text{CS}}$	39	$\overline{\text{WE}}$
3	I/O15	38	$\overline{\text{UB}}$
4	I/O14	37	$\overline{\text{LB}}$
5	I/O13	36	A14
6	I/O12	35	A13
7	I/O11	34	A12
8	I/O10	33	A11
9	I/O9	32	A10
10	I/O8	31	A9
11	GND	30	GND
12	I/O7	29	A8
13	I/O6	28	A7
14	I/O5	27	A6
15	I/O4	26	A5
16	I/O3	25	A4
17	I/O2	24	A3
18	I/O1	23	A2
19	I/O0	22	A1
20	$\overline{\text{OE}}$	21	A0

A0-A15	Addresses
I/O0-I/O15	Data Input/Output
$\overline{\text{CS}}$	Chip Select
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{UB}}$	Upper Byte Control
$\overline{\text{LB}}$	Lower Byte Control
VCC	Power
GND	Ground



Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage(1)	V_{CC}	4.5	5.5	V
Input HIGH Voltage	V_{IH}	2.2	V_{CC}+0.5	V
Input LOW Voltage	V_{IL}	-0.5	0.8	V
Operating Temp. Mil.	T_C	-55	125	°C
Operating Temp. Ind.	T_C	-40	85	°C
Operating Temp. Comm.	T_C	0	70	°C

Absolute Maximum Ratings (2)

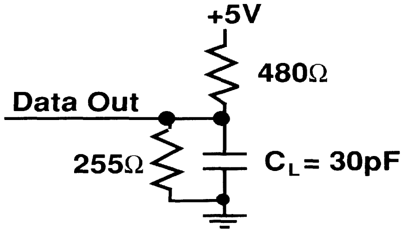
Temperature Under Bias	-55 °C to 125 °C
Storage Temperature	-65 °C to 150 °C
Supply Voltage(1)	-0.5V to 7.0 V
Signal Voltage On Any Pin	-0.5 V to V_{CC} + 0.5V
Power Dissipation	1 Watt
D.C. Continuous Output Current Per Output	20 mA
Lead Temperature (Soldering 10 sec)	260 °C

Notes:

1. All voltages referenced to V_{SS} (GND).

2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Load Test Circuits



C_L = 5pF for t_{CLZ} , t_{CHZ} , t_{BLZ} , t_{BHZ}, t_{OLZ}, t_{OHZ} , t_{WLZ}, t_{WHZ} .

Truth Table

Mode	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	X	X	High Z	I_{SB}
Standby	L	H	H	X	X	High Z	I_{SB}
Standby	≥ V_{CC} - 0.2 V	≥ V_{CC} - 0.2 V	≥ V_{CC} - 0.2 V	X	X	High Z	I_{FSB}
Read	L	L	L	L	H	Data Out	I_{CC2}
Write	L	L	L	X	L	Data In	I_{CC2}

Memory Scale

Access Time	55	70	85	100	120	Unit
S64K16	18	14	12	10	8	kbits/ns

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

DC and Operating Characteristics

M=Military; C=Commercial; I=Industrial

Parameters	Symbol	Test Conditions		S64K16 Min	S64K16 Max	S64K16L Min	S64K16L TYP 5V, 25°C	S64K16L Max	UNITS
Input Leakage	$\|I_{LI}\|$	V_{CC} = max, V_{IN} = GND to V_{CC}			2			2	uA
Output Leakage	$\|I_{LO}\|$	V_{OUT} = GND to V_{CC}, $\overline{CS} \geq V_{IH}$			2			2	uA
Static Supply Current	I_{CC1}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$ No Address Transitions	C I M		150 160 170		100	135 145 155	mA
Dynamic Supply Current	I_{CC2}	$\overline{CS} \leq V_{IL}$, $\overline{OE} = V_{IH}$ Address Change every t_{RC}			175		115	160	mA
Standby Supply Current with TTL Inputs	I_{SB}	$\overline{CS}$, $\overline{UB}$, $\overline{LB} \geq V_{IH}$ Address Change every t_{RC}	C I M		10 15 20		1.3	4 6 10	mA
Standby Supply Current with CMOS inputs	I_{FSB}	$\overline{CS}$, $\overline{UB}$, $\overline{LB} = V_{CC} \pm 0.2V$ No Address Transitions	C I M		NA NA NA		0.1	2 3 6	mA
Data Retention Current	I_{CCDR}	$\overline{CS}$, $\overline{UB}$, $\overline{LB} = V_{DR}$ min $V_{CC} = V_{DR}$ min	C I M		NA NA NA		10μA Vcc=2V	0.15 0.5 1.5	mA
Data Retention Voltage	V_{DR}	V_{CC} input voltage		NA		2.0			V
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.4			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA		2.4		2.4			V

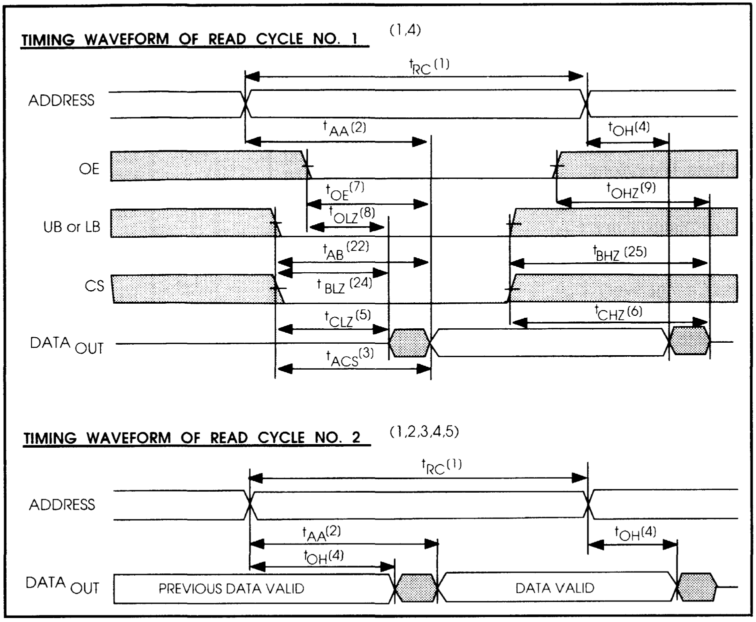
Pin Capacitance (Typical)	Test Conditions	Addresses	Data I/O	$\overline{UB}$, $\overline{LB}$, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$	Units
	Pin Voltage = 0V, ƒ=1.0 Mhz	8	10	16	pF

AC Characteristics (1)

No.	Parameter	Symbol	45C Min	45C Max	55 C,I, M Min	55 C,I, M Max	70 C,I,M Min	70 C,I,M Max	85 C,I,M Min	85 C,I,M Max	100 C,I,M Min	100 C,I,M Max	120 I,M Min	120 I,M Max
1	Read Cycle Time	t_{RC}	45		55		70		85		100		120	
2	Address Access Time	t_{AA}		45		55		70		85		100		120
3	$\overline{CS}$ Access Time	t_{ACS}		50		55		70		85		100		120
4	Output Hold from Address Change	t_{OH}	5		5		5		5		5		5	
5	$\overline{CS}$ Asserted to Output in Low Z	t_{CLZ} (2,3)	5		5		5		5		5		5	
6	$\overline{CS}$ Deasserted to Output in High Z	t_{CHZ} (2,3)	0	20	0	35	0	35	0	35	0	35	0	35
7	$\overline{OE}$ Asserted to Output Valid	t_{OE}		20		20		25		30		50		50
8	$\overline{OE}$ Asserted to Output in Low Z	t_{OLZ} (2,3)	0		0		0		0		0		0	
9	$\overline{OE}$ Asserted to Output in High Z	t_{OHZ} (2,3)	0	20	0	35	0	35	0	35	0	35	0	35
10	Write Cycle Time	t_{WC}	45		55		70		85		100		120	
11	Address Setup Time	t_{AS}	0		0		0		0		0		0	
12	Write Pulse Width	t_{WP}	30		35		35		40		45		50	
13	Write Recovery Time	t_{WR}	5		5		5		5		5		5	
14	Data Hold Time	t_{DH}	3		3		3		3		3		3	
15	Data Valid to End of Write	t_{DW}	25		25		30		35		40		40	
16	Output Active from End of Write	t_{WLZ} (2,3)	5		5		5		5		5		5	
17	$\overline{WE}$ Asserted to Output in High Z	t_{WHZ} (2,3)	0	20	0	35	0	35	0	35	0	35	0	35
18	Chip Deselect to Data Retention Time	t_{CDR} (2)	0		0		0		0		0		0	
19	Operation Recovery Time	t_R (2)		45		55		70		85		100		120
20	$\overline{CS}$ Asserted to End of Write	t_{CW}	35		45		60		75		75		75	
21	Address Valid to End of Write	t_{AW}	35		45		60		75		75		75	
22	$\overline{UB}/\overline{LB}$ Byte Enable Access Time	t_{AB}		45		55		70		85		100		120
23	$\overline{UB}/\overline{LB}$ Byte Enable to End of Write	t_{BW}	35		45		60		75		75		75	
24	$\overline{UB}/\overline{LB}$ Byte Enable to Output in Low Z	t_{BLZ} (2,3)	5		5		5		5		5		5	
25	$\overline{UB}/\overline{LB}$ Byte Enable to Output in High Z	t_{BHZ} (2,3)	0	20	0	35	0	35	0	35	0	35	0	35

Notes: (1) At Recommended Operating Conditions. All Values in Nanoseconds. (2) This Parameter is characterized initially and after any design or process change which could affect it. It is guaranteed to, but not tested to, the limits specified. (3) All I/O Transitions are measured ± 500mV from steady state with loading as specified in "Load Test Circuits."

READ CYCLE



Reading the S64K16 device is accomplished by taking chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and output enable($\overline{OE}$) LOW , while write enable ($\overline{WE}$) remains inactive or high. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

Notes:

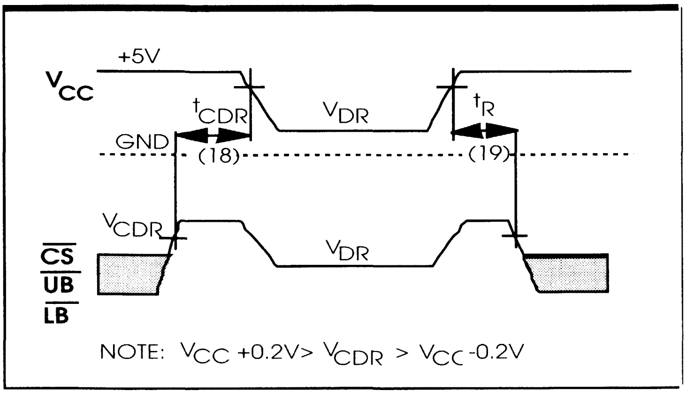
1. $\overline{WE}$ is high for READ CYCLES.
2. Device is continuously selected, $\overline{CS}$= V_{IL} and $\overline{UB}$, $\overline{LB}$ = V_{IL} for 16 outputs active.
3. $\overline{OE}$ = V_{IL}.
4. Data Output transitions measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
5. $\overline{UB}$ or $\overline{LB}$ = V_{IL}.

Data Retention Cycle

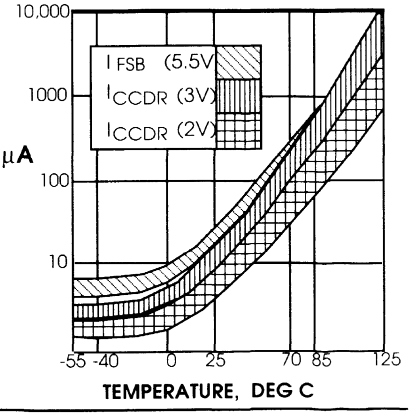
S64K16 devices exhibit very low current drain when operated in Data Retention Mode. This Mode is entered by first driving Chip Select to V_{CC} and subsequently driving both V_{CC} and Chip Select to V_{DR}. Chip Select must be set up before the V_{CC} drops below its minimum level. When exiting from Data Retention Mode, the user must wait one full Read Cycle Time prior to asserting Chip Select.

The curve showing typical device current is included to assist the user in understanding the relationship of the current required by the part when its Temperature and Voltage vary. The device is tested and guaranteed to conditions specified under DC and Operating Conditions.

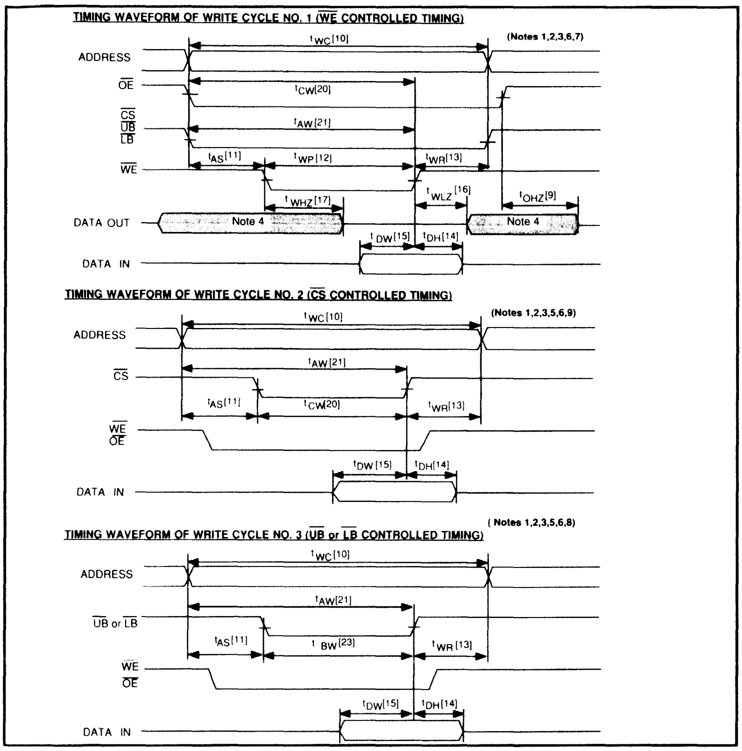
DATA RETENTION MODE TIMING



Standby Current, Typical



WRITE CYCLE



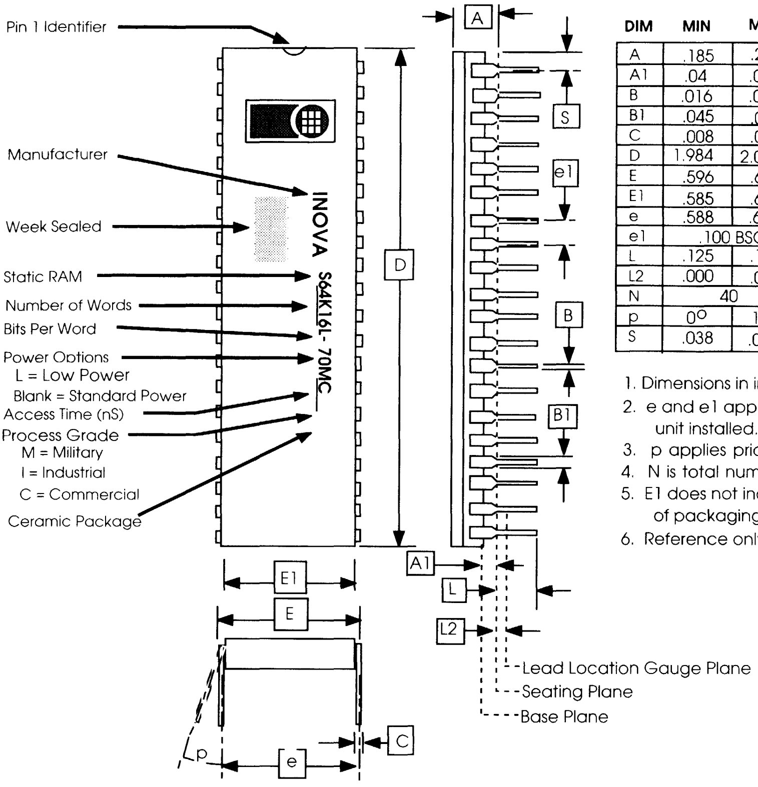
Writing to the S64K16 is achieved when the chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and write enable ($\overline{WE}$) inputs are LOW. Data on the input/output pins of the selected byte (I/O8 - I/O15, I/O0 - I/O7) is written into the memory location specified on the address pins (A0-A15).

The input/output pins remain in a high impedance state when chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$), or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

Notes:

1. $\overline{WE}$ or $\overline{CS}$ or both $\overline{UB}$ and $\overline{LB}$ must be high during all address transitions.
2. A write occurs during the overlap (TWP) of a low $\overline{CS}$, $\overline{UB}$, $\overline{LB}$ and a low $\overline{WE}$.
3. TWR is measured from the earlier of $\overline{CS}$, $\overline{UB}$, $\overline{LB}$, or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$, or $\overline{UB}$ and $\overline{LB}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Data output transitions are measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse low is ≥TDW +TWHZ to allow the I/O drivers to turn off and data to be placed on the the bus for the required TDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified TWP.
8. $\overline{CS}$ held low.
9. $\overline{UB}$ and $\overline{LB}$ held low.

Package Dimension and Ordering Information



DIM	MIN	MAX	NOTE
A	.185	.230	
A1	.04	.06	
B	.016	.020	
B1	.045	.055	
C	.008	.012	
D	1.984	2.016	
E	.596	.624	
E1	.585	.605	
e	.588	.612	2
e1	.100 BSC		2
L	.125	.170	
L2	.000	.003	2
N	40		4
p	0°	15°	3
S	.038	.062	6

1. Dimensions in inches
2. e and e1 apply in zone L2 with unit installed.
3. p applies prior to installation.
4. N is total number of terminals.
5. E1 does not include particles of packaging materials.
6. Reference only.

S64K16X·45XX

C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (-40°C to 85°C)
M = Military Temperature Range (-55°C to 125°C)

C = 600 mil Ceramic Sidebrazed DIP

L suffix on base part number = Low Power Device

Printed in U.S.A., AMN-790

inova microelectronics *S256K4*

Preliminary Data

256K x 4 Static RAM

Key Parameters *S256K4 and S256K4L*	*Device Types*			*Unit*
	25C	*35M* *35I* *35C*	*45M* *45I* *45C*	
Access Time	25	35	45	nS
Cycle Time	25	35	45	nS
Output Enable Access	10	15	20	nS

Features

- **300 mil wide 28 pin DIP**
- **Advanced 4-T CMOS technology**
- **SOJ, LCC, and Flatpack Available**
- **Military, industrial, and commercial temperature range**
- **Military grades compliant to MIL-STD-883C**

General Description

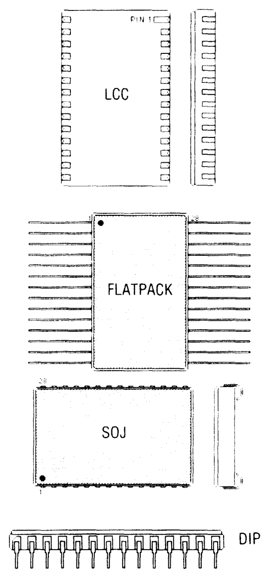
The Inova S256K4 is a high performance one megabit Static Random Access Memory (SRAM) organized as 256K by four bits.

The S256K4 is manufactured using a highly reliable, four transistor cell CMOS process. This provides a component which combines low active and standby power characteristics with high performance.

All inputs are fully TTL-compatible. Operation is fully static, without need for extra control logic to generate clock signals.

Every military grade device is fully compliant to MIL-STD-883C, paragraph 1.2.1. Industrial and commercial grade devices are fabricated in the same production line which ensures that they are also of the highest quality.

Package Options



Pinout

1	**A10**	28	**VCC**
2	**A9**	27	**A11**
3	**A8**	26	**A12**
4	**A7**	25	**A13**
5	**A6**	24	**A14**
6	**A5**	23	**A15**
7	**A4**	22	**A16**
8	**A3**	21	**A17**
9	**A2**	20	**NC**
10	**A1**	19	**I/O3**
11	**A0**	18	**I/O2**
12	**$\overline{\text{CS}}$**	17	**I/O1**
13	**$\overline{\text{OE}}$**	16	**I/O0**
14	**VSS**	15	**WE**

A0-A17	Address Inputs
I/O0-I/O3	Data Input/ Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{CS}}$	Chip Select
VCC	+5V Power
VSS	Ground

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage(1)	V_{CC}	4.5	5.5	V
Input HIGH Voltage	V_{IH}	2.2	V_{CC}+0.5	V
Input LOW Voltage	V_{IL}	-0.5	0.8	V
Operating Temp. Mil.	T_C	-55	125	°C
Operating Temp. Ind.	T_C	-40	85	°C
Operating Temp. Comm.	T_C	0	70	°C

Absolute Maximum Ratings (2)

Temperature Under Bias	-55 °C to 125 °C
Storage Temperature	-65 °C to 150 °C
Supply Voltage(1)	-0.5V to 7.0 V
Signal Voltage On Any Pin	-0.5 V to V_{CC} + 0.5V
Power Dissipation	1 Watt
D.C. Continuous Output Current Per Output	20 mA
Lead Temperature (Soldering 10 sec)	260 °C

Notes:

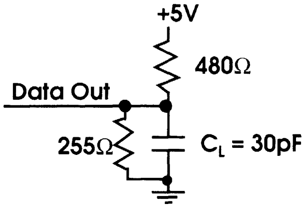
1. All voltages referenced to V_{SS} (GND).

2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	High Z	I_{SB}/I_{FSB}
Read	L	L	H	Output	I_{CC2}
Write	L	X	L	Input	I_{CC2}
Output Disable	L	H	H	High Z	I_{CC2}

Load Test Circuits



C_L = 5pF for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{WLZ}.

Memory Scale

Access Time	25	35	45	Unit
S256K4	40	29	22	kbits/ns

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

DC and Operating Characteristics

M=Military; C=Commercial; I=Industrial

Parameters	Symbol	Test Conditions		S256K4 Min	S256K4 Max	S256K4L Min	S256K4L Max	UNITS
Input Leakage	$\lvert I_{LI} \rvert$	V_{CC} = max, V_{IN} = GND to V_{CC}			2		2	µA
Output Leakage	$\lvert I_{LO} \rvert$	V_{OUT} = GND to V_{CC}, $\overline{CS} > V_{IH}$			2		2	µA
Static Supply Current	I_{CC1}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$ No Address Transitions	C I M		90 95 100		80 85 90	mA
Dynamic Supply Current	I_{CC2}	$\overline{CS} \le V_{IL}$, $\overline{OE} = V_{IH}$ Address change every t_{RC}			140		125	mA
Standby Supply Current With Address Changes	I_{SB}	$\overline{CS} > V_{IH}$ Address change every t_{RC}	C I M		30 35 40		3 4 10	mA
Standby Supply Current With CMOS Levels	I_{FSB}	$\overline{CS} = V_{CC} \pm 0.2V$ No Address Transistions	C I M				0.75 1.25 5.0	mA
Data Retention Current At V = 2.0V_{DR}	I_{CCDR}	$\overline{CS} = V_{DR}$ min $V_{CC} = V_{DR}$ min	C I M				0.10 0.15 2.0	mA
Data Retention Voltage	V_{DR}	V_{CC} input voltage		3.0		2.0		V
Output Low Voltage	V_{OL}	I_{OL} = 8 mA			0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA		2.4		2.4		V

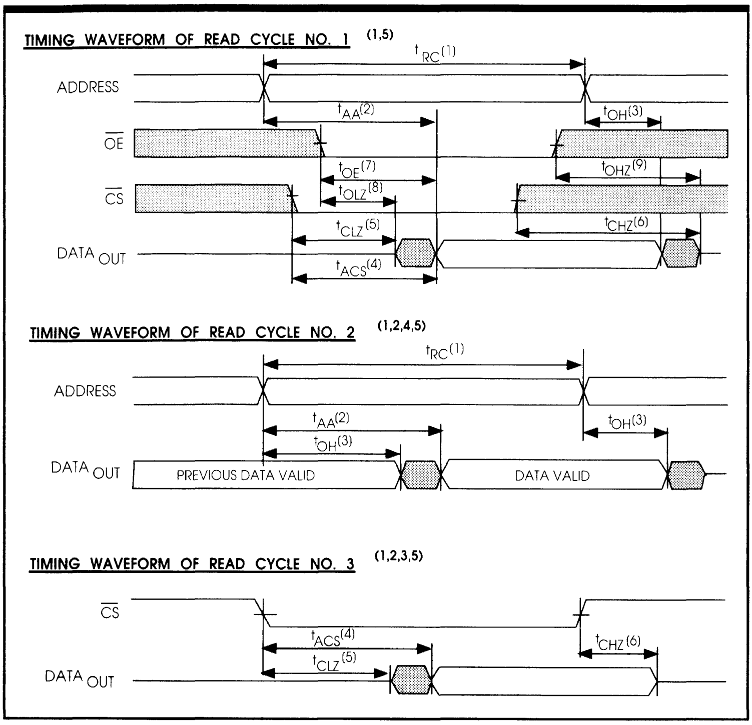
Pin Capacitance (Typical)	Test Conditions	Addresses	Data I/O	$\overline{CS}$, $\overline{WE}$, $\overline{OE}$	Units
	Pin Voltage = 0V, f=1.0 Mhz	8	10	12	pF

AC Characteristics (1)

No.	S256K4 and S256K4L Parameter	Symbol	25C Min	25C Max	35C,I,M Min	35C,I,M Max	45C,I,M Min	45C,I,M Max
1	Read Cycle Time	t_{RC}	25		35		45	
2	Address Access Time	t_{AA}		25		35		45
3	Output Hold from Address Change	t_{OH}	3		5		5	
4	$\overline{CS}$ Access Time	t_{ACS}		25		35		45
5	$\overline{CS}$ on to Output in Low Z	t_{CLZ} (2,3)	5		5		5	
6	$\overline{CS}$ off to Output in High Z	t_{CHZ} (2,3)	0	10	0	15	0	20
7	$\overline{OE}$ on to Output Valid	t_{OE}		10		15		20
8	$\overline{OE}$ on to Output in Low Z	t_{OLZ} (2,3)	0		0		0	
9	$\overline{OE}$ off to Output in High Z	t_{OHZ} (2,3)	0	10	0	15	0	20
10	Write Cycle Time	t_{WC}	25		35		45	
11	Chip Selection to End of Write	t_{CW}	20		25		30	
12	Address Valid to End of Write	t_{AW}	20		25		30	
13	Address Set-up Time	t_{AS}	0		0		0	
14	Write Pulse Width	t_{WP}	20		25		30	
15	Write Recovery Time	t_{WR}	0		0		0	
16	Data Valid Set-Up to End of Write	t_{DW}	15		20		25	
17	Data Hold from End of Write	t_{DH}	0		0		0	
18	Write Pulse on to Output in High Z	$t_{WHZ(2,3)}$	0	10	0	15	0	20
19	Write Pulse off to Output in Low Z	$t_{WLZ(2,3)}$	5		5		5	
20	Chip Deselect to Data Retention	$t_{CDR(2)}$	0		0		0	
21	Operation Recovery Time	t_{R} (2)		25		35		45

Notes: (1) At Recommended Operating Conditions. All Values in Nanoseconds. (2) This Parameter is characterized initially and after any design or process change which could affect it. It is guaranteed to, but not tested to, the limits specified. (3) All I/O Transitions are measured ± 500mV from steady state with loading as specified in "Load Test Circuits."

READ CYCLE



Reading the S256K4 device is accomplished by taking chip select (CS) and output enable(OE) LOW, while write enable (WE) remains inactive or high. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/ output pins.

Notes:

1. WE is high for READ CYCLES.

2. Device is continuously selected, CS= V_{IL} for all outputs active.

3. Address valid prior to or coincident with CS transition low.

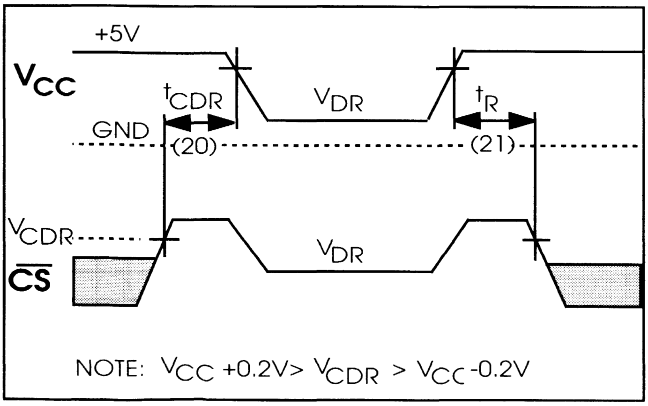
4. OE =V_{IL}

5. Data Output transitions measured ±500mV from steady state. This parameter is sampled and not 100% tested

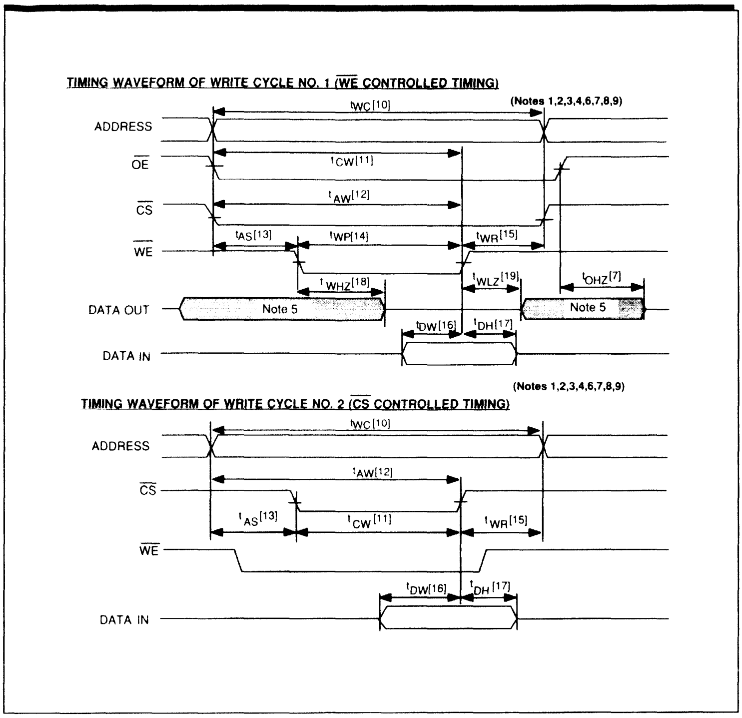
Data Retention

S256K4 devices exhibit very low current drain when operated in Data Retention Mode. This Mode is entered by first driving Chip Select to V_{CC} and subsequently driving both V_{CC} and Chip Select to V_{DR}. Chip Select must be set up before the V_{CC} drops below its minimum level. When exiting from Data Retention Mode, the user must wait one full Read Cycle Time prior to asserting Chip Select.

DATA RETENTION TIMING



WRITE CYCLE



Writing to the S256K4 is achieved when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are LOW. Data on the input/output pins is written into the memory location specified on the address pins (A0-A17).

The input/output pins remain in a high impedance state when chip select ($\overline{CS}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

NOTES

1. **A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition of $\overline{CS}$ going low and $\overline{WE}$ going low. A write ends at the earliest transition of $\overline{CS}$ going high and $\overline{WE}$ going high. During a $\overline{WE}$ controlled write cycle, write pulse low is ≥ TDW + TWHZ to allow the I/O drivers to turn off and data to be placed on the bus for the required TDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle this requirement does not apply and the write pulse can be as short as the specified TWP.**

2. **TCW is measured from $\overline{CS}$ going low to the end of write.**

3. **TAS is measured from the address valid to the beginning of write.**

4. **TWR is measured from the earliest of $\overline{CS}$ or $\overline{WE}$ going high to the end of write.**

5. **During this period, I/O pins are in the output state, therefore input signals of opposite phase must not be applied.**

6. **If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ goes low, the outputs remain in a high impedance state.**

7. **DATA OUT is the same data written during the present cycle.**

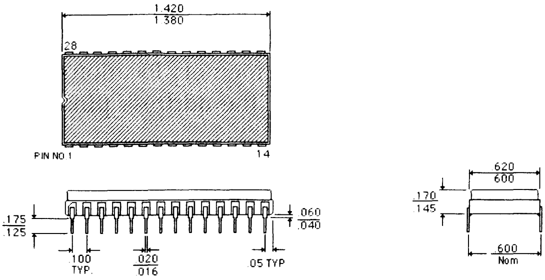
8. **The real data of the next address is present at DATA OUT TAA after the address transition.**

9. **The tri-state parameters of data input and output are measured ±500mV from steady state. These parameters are sampled and characterized but not 100% tested.**

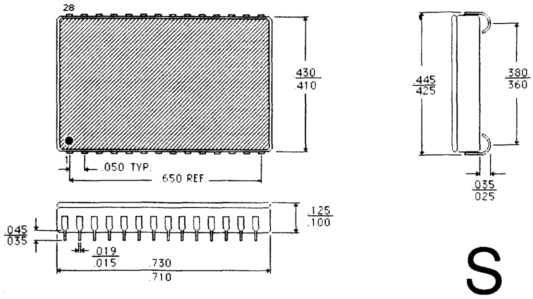
Package Dimension and Ordering Information

C

28 PIN CERAMIC SIDEBRAZED DUAL-IN-LINE PACKAGE 600 MILWIDE



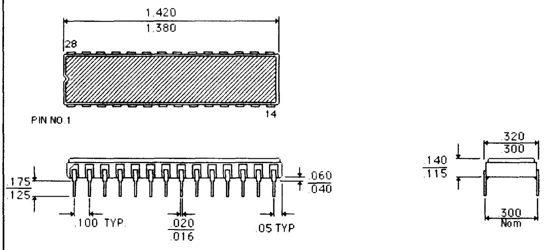
28 PIN CERAMIC "J" LEADED 400 MIL WIDE PACKAGE



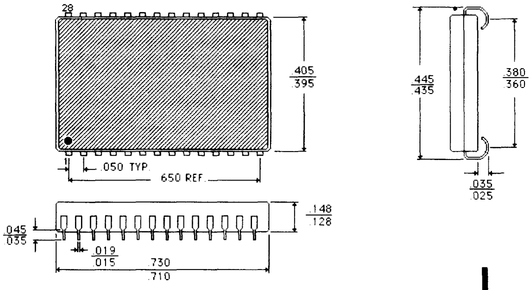
S

T

28 PIN CERAMIC SIDEBRAZED DUAL-IN-LINE PACKAGE 300 MIL WIDE



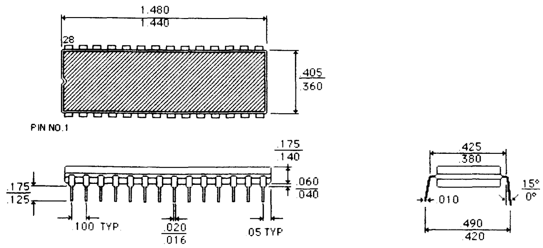
28 PIN PLASTIC SOJ PACKAGE,400 MIL WIDE BODY



J

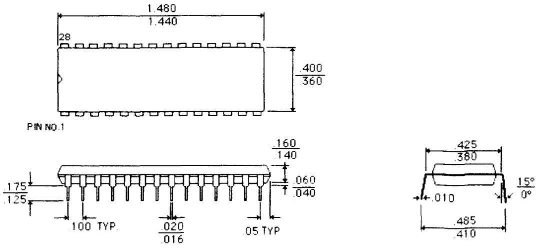
D

28 LEAD (400 MIL) CERDIP PACKAGE



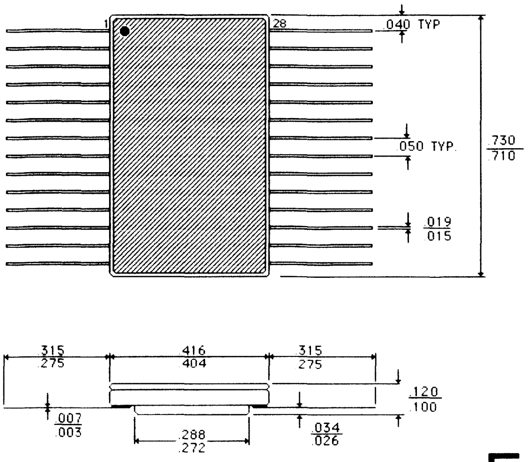
P

28 LEAD (400 MIL) MOLDED DIP PACKAGE



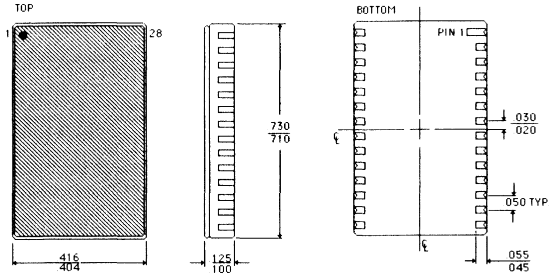
Package Dimension and Ordering Information

28 PIN CERAMIC FLATPACK,400 MIL WIDE PACKAGE



F

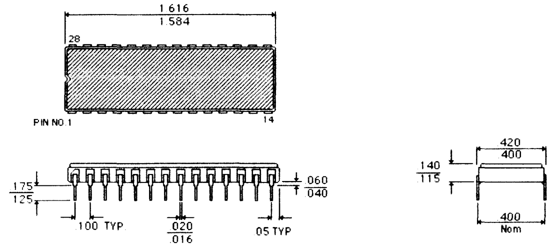
28 PIN LEADLESS CHIP CARRIER PACKAGE



L

E

28 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
400 MIL WIDE



S256K4X·45XX

C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (-40°C to 85°C)
M = Military Temperature Range (-55°C to 125°C)

C = 600 mil Ceramic Sidebrazed DIP
D = 400 mil CERDIP
E = 400 mil Ceramic Sidebrazed DIP
T = 300 mil Ceramic Sidebrazed DIP
P = 400 mil Plastic DIP
F = Flatpack
S = Ceramic SOJ
J = Plastic SOJ
L = Leadless Chip Carrier

L suffix on base part number =
Low Power Device

All Specifications are subject to change without notice.
Printed in U.S.A., AMN-790

inova microelectronics

S1M1

Preliminary Data

1M x 1 Static RAM

Key Parameters	***Device Types***			
S1M1 and S1M1L	***25C***	***35M 35I 35C***	***45M 45I 45C***	***Unit***
Access Time	25	35	45	nS
Cycle Time	25	35	45	nS
Output Enable Access	10	15	20	nS

Features

- **300 mil 28 pin DIP**
- **Advanced 4-T CMOS technology**
- **SOJ, LCC, and Flatpack Available**
- **Military, industrial, and commercial temperature range**
- **Military grades compliant to MIL-STD-883C**

General Description

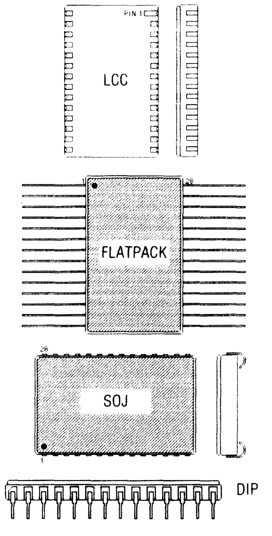
The Inova S1M1 is a high performance one megabit Static Random Access Memory (SRAM) organized as 1,024 K by one bit.

The S1M1 is manufactured using a highly reliable, four transistor cell CMOS process. This provides a component which combines low active and standby power characteristics with high performance.

All inputs are fully TTL-compatible. Operation is fully static, without need for extra control logic to generate clock signals.

Every military grade device is fully compliant to MIL-STD-883C, paragraph 1.2.1. Industrial and commercial grade devices are fabricated in the same production line which assures that they are also of the highest quality.

Package Options



Pinout

1	**A9**	28	**VCC**
2	**A8**	27	**A1**
3	**A7**	26	**A11**
4	**A6**	25	**A12**
5	**A5**	24	**A13**
6	**A4**	23	**A14**
7	**NC**	22	**A15**
8	**A3**	21	**NC**
9	**A2**	20	**A16**
10	**A1**	19	**A17**
11	**A0**	18	**A18**
12	**D-OUT**	17	**A19**
13	**WE**	16	**D-IN**
14	**VSS**	15	**$\overline{\text{CS}}$**

A0-A19	Address Inputs
D-In	Data Input
D-Out	Data output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CS}}$	Chip Select
VCC	+5V Power
VSS	Ground

Recommended Operating Conditions

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*
Supply Voltage[1]	V_{CC}	4.5	5.5	V
Input HIGH Voltage	V_{IH}	2.2	V_{CC}+0.5	V
Input LOW Voltage	V_{IL}	-0.5	0.8	V
Operating Temp. Mil.	T_C	-55	125	°C
Operating Temp. Ind.	T_C	-40	85	°C
Operating Temp. Comm.	T_C	0	70	°C

Absolute Maximum Ratings (2)

Temperature Under Bias	-55 °C to 125 °C
Storage Temperature	-65 °C to 150 °C
Supply Voltage[1]	-0.5V to 7.0 V
Signal Voltage On Any Pin	-0.5 V to V_{CC} + 0.5V
Power Dissipation	1 Watt
D.C. Continuous Output Current Per Output	20 mA
Lead Temperature (Soldering 10 sec)	260 °C

Notes:

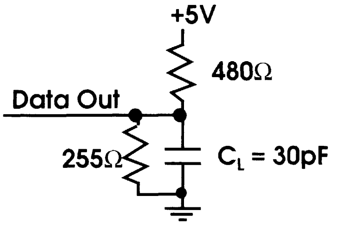
1. All voltages referenced to V_{SS} (GND).

2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Truth Table

Mode	*$\overline{CS}$*	*$\overline{WE}$*	*I/O Operation*	*Supply Current*
Standby	H	X	High Z	I_{SB} - I_{FSB}
Read	L	H	Data Out	I_{CC}
Write	L	L	Input	I_{CC}

Load Test Circuits



C_L = 5pF for t_{WLZ}, t_{WHZ}, t_{CLZ}, t_{CHZ}.

Memory Scale

Access Time	25	35	45	**Unit**
S1M1	40	29	22	kbits/ns

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

DC and Operating Characteristics

M=Military; C=Commercial; I=Industrial

Parameters	Symbol	Test Conditions		S1M1 Min	S1M1 Max	S1M1L Min	S1M1L Max	UNITS
Input Leakage	$\lvert I_{LI} \rvert$	V_{CC} = max, V_{IN} = GND to V_{CC}			2		2	µA
Output Leakage	$\lvert I_{LO} \rvert$	V_{OUT} = GND to V_{CC}, $\overline{CS}$ > V_{IH}			2		2	µA
Static Supply Current	I_{CC1}	$\overline{CS}$ = V_{IL} No Address Transitions	C I M		90 95 100		80 85 90	mA
Dynamic Supply Current	I_{CC2}	$\overline{CS}$ ≤ V_{IL} Address change every t_{RC}			140		125	mA
Standby Supply Current With TTL Levels	I_{SB}	$\overline{CS}$>V_{IH} Address change every t_{RC}	C I M		30 35 40		3 4 10	mA
Standby Supply Current With CMOS Levels	I_{FSB}	$\overline{CS}$ = V_{CC} ± 0.2V No Address Transitions	C I M				0.75 1.25 5.0	mA
Data Retention Current At V_{DR} = 2.0V	I_{CCDR}	$\overline{CS}$ = V_{DR} min V_{CC} = V_{DR} min	C I M				0.10 0.15 2.0	mA
Data Retention Voltage	V_{DR}	V_{CC} input voltage		3.0		2.0		V
Output Low Voltage	V_{OL}	I_{OL} = 8 mA			0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA		2.4		2.4		V

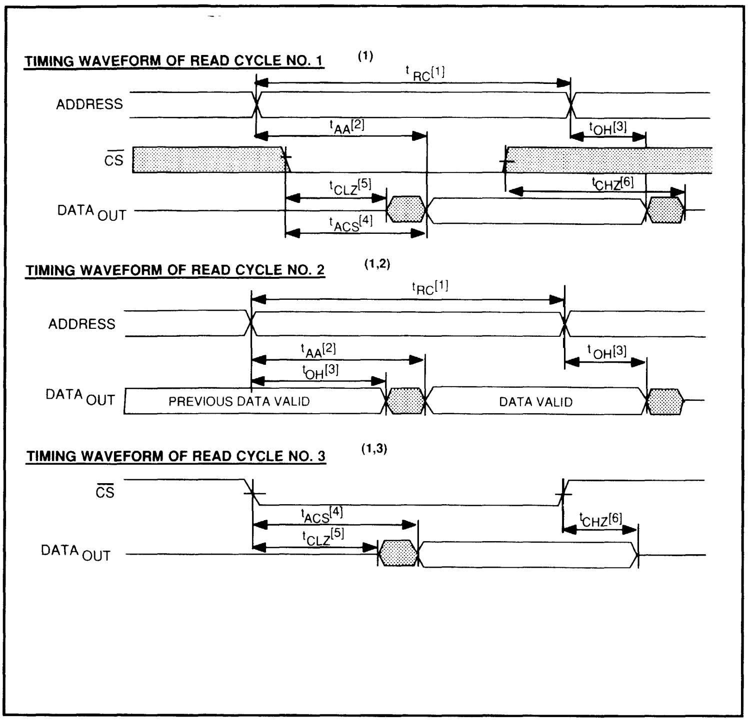
Pin Capacitance (Typical)	Test Conditions	Addresses	Data I/O	$\overline{CS}$, $\overline{WE}$	Units
	Pin Voltage = 0V, f=1.0 Mhz	8	10	12	pF

AC Characteristics (1)

No.	S1M1 and S1M1L Parameter	Symbol	25C Min	25C Max	35C,I,M Min	35C,I,M Max	45C,I,M Min	45C,I,M Max
1	Read Cycle Time	t_{RC}	25		35		45	
2	Address Access Time	t_{AA}		25		35		45
3	Output Hold from Address Change	t_{OH}	3		5		5	
4	$\overline{CS}$ Access Time	t_{ACS}		25		35		45
5	$\overline{CS}$ on to Output in Low Z	$t_{CLZ(2,3)}$	5		5		5	
6	$\overline{CS}$ off to Output in High Z	$t_{CHZ(2,3)}$	0	10	0	15	0	20
7	Write Cycle Time	t_{WC}	25		35		45	
8	Chip Selection to End of Write	t_{CW}	20		25		30	
9	Address Valid to End of Write	t_{AW}	20		25		30	
10	Address Set-up Time	t_{AS}	0		0		0	
11	Write Pulse Width	t_{WP}	20		25		30	
12	Write Recovery Time	t_{WR}	0		0		0	
13	Data Valid Set-Up to End of Write	t_{DW}	15		20		25	
14	Data Hold from End of Write	t_{DH}	0		0		0	
15	Write Pulse on to Output in High Z	$t_{WHZ(2,3)}$	0	10	0	15	0	20
16	Write Pulse off to Output in Low Z	$t_{WLZ(2,3)}$	5		5		5	
17	Chip Deselect to Data Retention	$t_{CDR(2)}$	0		0		0	
18	Operation Recovery Time	$t_{R(2)}$		25		35		45

Notes: (1) At Recommended Operating Conditions. All Values in Nanoseconds. (2) This Parameter is characterized initially and after any design or process change which could affect it. It is guaranteed to, but not tested to, the limits specified. (3) All I/O Transitions are measured ± 500mV from steady state with loading as specified in "Load Test Circuits."

READ CYCLE


TIMING WAVEFORM OF READ CYCLE NO. 1 (1)

TIMING WAVEFORM OF READ CYCLE NO. 2 (1,2)

TIMING WAVEFORM OF READ CYCLE NO. 3 (1,3)

Reading the S1M1 device is accomplished by taking chip select (CS) low , while write enable (WE) remains inactive or high. Under these conditions, the content of the memory location specified by the address pins will appear on the output pin.

Notes:

1. $\overline{WE}$ is high for READ CYCLES.

2. Device is continuously selected, $\overline{CS}$= V_{IL} for all outputs active.

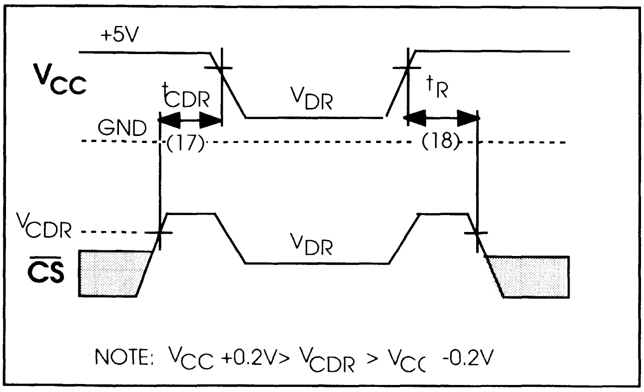
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

5. Data Output transitions measured ±500mV from steady state. This parameter is sampled and not 100% tested

Data Retention

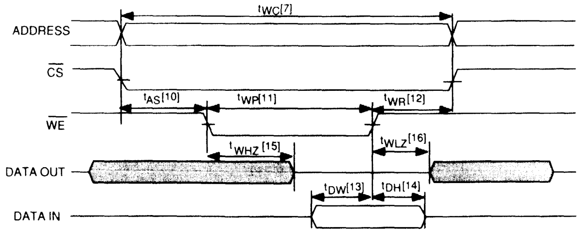
S1M1 devices exhibit very low current drain when operated in Data Retention Mode. This Mode is entered by first driving Chip Select to V_{CC} and subsequently driving both V_{CC} and Chip Select to V_{DR}. Chip Select must be set up before the V_{CC} drops below its minimum level. When exiting from Data Retention Mode, the user must wait one full Read Cycle Time prior to asserting Chip Select.

DATA RETENTION TIMING

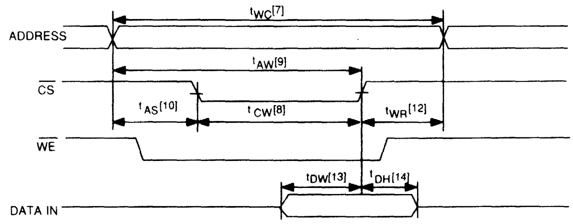


NOTE: V_{CC} +0.2V> V_{CDR} > V_{CC} -0.2V

WRITE CYCLE



TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{\text{WE}}$ CONTROLLED TIMING) (Notes 1,2,3,4,5,6,7,8)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ CONTROLLED TIMING) (Notes 1,2,3,4,5,6,7,8)

Writing to the S1M1 is achieved when the chip select ($\overline{\text{CS}}$) and write enable ($\overline{\text{WE}}$) inputs are low. Data on the input pin is written into the memory location specified on the address pins (A0-A19).

The output pin remains in a high impedance state when chip select ($\overline{\text{CS}}$) is high, or write enable ($\overline{\text{WE}}$) is low.

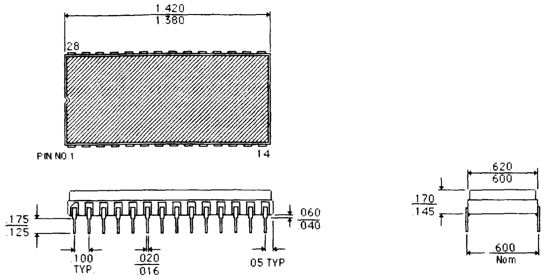
NOTES:

1. A Write occurs duringthe overlap of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$. A write begins at the latest transition of $\overline{\text{CS}}$ going low and $\overline{\text{WE}}$ going low. A write ends at the earliest transition of either $\overline{\text{CS}}$ going high or $\overline{\text{WE}}$ going high.
2. TCW is measured from $\overline{\text{CS}}$ going low to the end of write.
3. TAS is measured from the address valid to the beginning of write.
4. TWR is measured from the earliest of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of write.
5. If $\overline{\text{CS}}$ goes low simultaneously with $\overline{\text{WE}}$ going low or after $\overline{\text{WE}}$ goes low, the outputs remain in a high impedance state.
6. DATA OUT is the same data written during the present cycle.
7. The real data of the next address is present at DATA OUT TAA after the address transition.
8. The tri-state parameters of data output are measured ±500 mV from steady state. These parameters are sampled but not 100% tested.

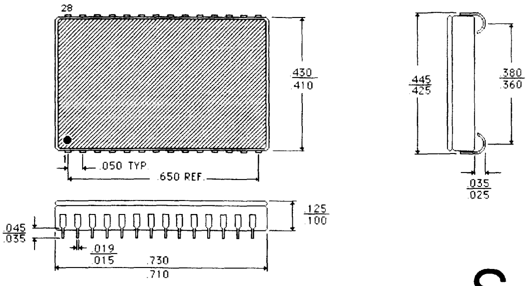
Package Dimension and Ordering Information

28 PIN CERAMIC SIDEBRAZED DUAL-IN-LINE PACKAGE 600 MILWIDE

C



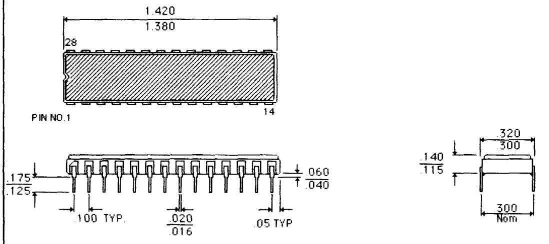
28 PIN CERAMIC "J" LEADED 400 MIL WIDE PACKAGE



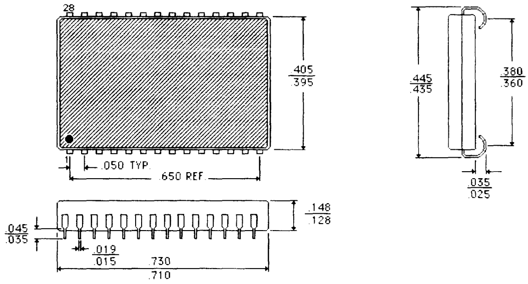
S

28 PIN CERAMIC SIDEBRAZED DUAL-IN-LINE PACKAGE 300 MIL WIDE

T



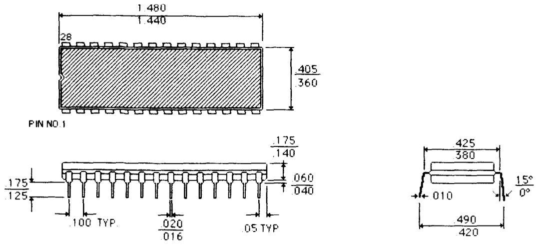
28 PIN PLASTIC SOJ PACKAGE,400 MIL WIDE BODY



J

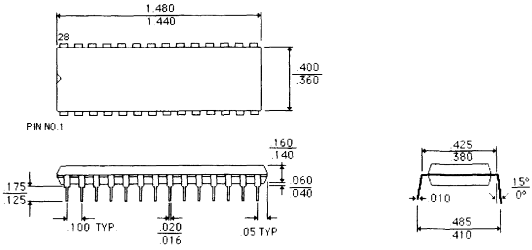
28 LEAD (400 MIL) CERDIP PACKAGE

D



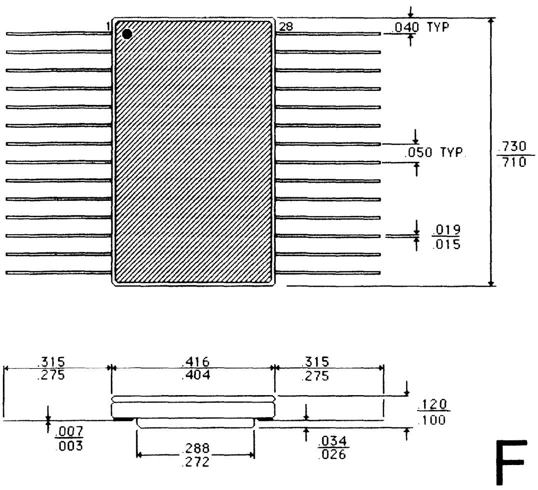
28 LEAD (400 MIL) MOLDED DIP PACKAGE

P



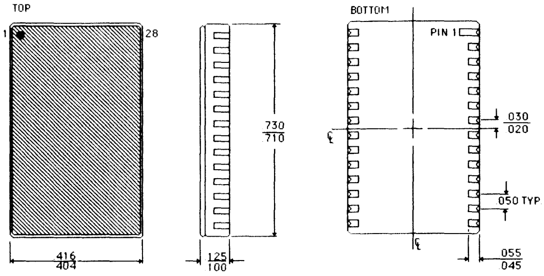
Package Dimension and Ordering Information

28 PIN CERAMIC FLATPACK,400 MIL WIDE PACKAGE



F

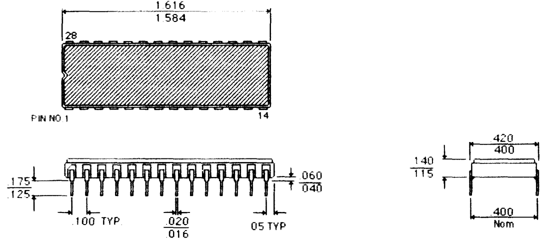
28 PIN LEADLESS CHIP CARRIER PACKAGE



L

28 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
400 MIL WIDE

E



S1M1X-45XX
X

- C = Commercial Temperature Range (0°C to 70°C)
- I = Industrial Temperature Range (-40°C to 85°C)
- M = Military Temperature Range (-55°C to 125°C)

- C = 600 mil Ceramic Sidebrazed DIP
- D = 400 mil CERDIP
- E = 400 mil Ceramic Sidebrazed DIP
- T = 300 mil Ceramic Sidebrazed DIP
- P = 400 mil Plastic DIP
- F = Flatpack
- S = Ceramic SOJ
- J = Plastic SOJ
- L = Leadless Chip Carrier

- L suffix on base part number = Low Power Device

All Specifications are subject to change without notice.
Printed in U.S.A., AMN-790

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inova

S512K8

Preliminary Data

512K x 8 Static RAM

Key Parameters	***Device Types***			
S512K8 and S512K8L	***45CC***	***55MC 55IC 55CC***	***70MC 70IC 70CC***	***Unit***
Access Time	45	55	70	nS
Cycle Time	45	55	70	nS
Output Enable Access	25	30	35	nS

Features

- **Advanced 4-T CMOS technology**
- **32 pin 600 mil DIP**
- **Monolithic**
- **Military, industrial, and commercial temperature range**
- **Military grades compliant to MIL-STD-883C**

General Description

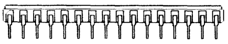
The Inova S512K8 is a high performance four megabit Static Random Access Memory (SRAM) organized as 512K eight -bit bytes.

The S512K8 is manufactured using a highly reliable, four transistor cell CMOS process. This provides a component which combines low active and standby power characteristics with high performance.

All inputs are fully TTL-compatible. Operation is fully static, without need for extra control logic to generate clock signals.

Every military grade device is fully compliant to MIL-STD-883C, paragraph 1.2.1. Industrial and commercial grade devices are fabricated in the same production line which assures that they are also of the highest quality.

Package Options



DIP

Pinout

1	**A18**	32	**VCC**
2	**A16**	31	**A15**
3	**A14**	30	**A17**
4	**A12**	29	**$\overline{\text{WE}}$**
5	**A7**	28	**A13**
6	**A6**	27	**A8**
7	**A5**	26	**A9**
8	**A4**	25	**A11**
9	**A3**	24	**$\overline{\text{OE}}$**
10	**A2**	23	**A10**
11	**A1**	22	**$\overline{\text{CS}}$**
12	**A0**	21	**I/O7**
13	**I/O0**	20	**I/O6**
14	**I/O1**	19	**I/O5**
15	**I/O2**	18	**I/O4**
16	**VSS**	17	**I/O3**

A0-A16	Address Inputs
I/O0-I/O7	Data Input/Output
WE	Write Enable
OE	Output Enable
CS	Chip Select
VCC	+5V Power
VSS	Ground

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage(1)	V_{CC}	4.5	5.5	V
Input HIGH Voltage	V_{IH}	2.2	V_{CC}+0.5	V
Input LOW Voltage	V_{IL}	-0.5	0.8	V
Operating Temp. Mil.	T_C	-55	125	°C
Operating Temp. Ind.	T_C	-40	85	°C
Operating Temp. Comm.	T_C	0	70	°C

Absolute Maximum Ratings (2)

Temperature Under Bias	-55 °C to 125 °C
Storage Temperature	-65 °C to 150 °C
Supply Voltage(1)	-0.5V to 7.0 V
Signal Voltage On Any Pin	-0.5 V to V_{CC} + 0.5V
Power Dissipation	1 Watt
D.C. Continuous Output Current Per Output	20 mA
Lead Temperature (Soldering 10 sec)	260 °C

Notes:

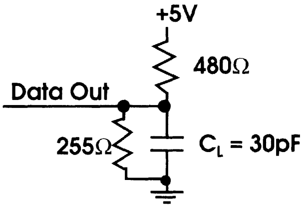
1. All voltages referenced to V_{SS} (GND).

2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	High Z	I_{SB}/I_{FSB}
Read	L	L	H	Output	I_{CC2}
Write	L	X	L	Input	I_{CC2}
Output Disable	L	H	H	High Z	I_{CC2}

Load Test Circuits



C_L = 5pF for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{WLZ}.

Memory Scale

Access Time	45	55	70	Unit
S512K8	89	73	57	kbits/ns

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

Preliminary Data

DC and Operating Characteristics

M=Military; C=Commercial; I=Industrial

Parameters	Symbol	Test Conditions		S512K8 Min	S512K8 Max	S512K8L Min	S512K8L TYP 5V, 25°C	S512K8L Max	UNITS
Input Leakage	$\lvert I_{LI} \rvert$	V_{CC} = max, V_{IN}= GND to V_{CC}				2		2	µA
Output Leakage	$\lvert I_{LO} \rvert$	V_{OUT} = GND to V_{CC} ,$\overline{CS} \geq V_{IH}$				2		2	µA
Static Supply Current	I_{CC1}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$ No Address Transitions	C I M			90 100 115		80 90 105	mA
Dynamic Supply Current	I_{CC2}	$\overline{CS} \leq V_{IL}$, $\overline{OE} = V_{IH}$ Address Change every t_{RC}				170		150	mA
Standby Supply Current with TTL Inputs	I_{SB}	$\overline{CS} \geq V_{IH}$ Address Change every t_{RC}	C I M			25 30 35		15 20 25	mA
Standby Supply Current with CMOS inputs	I_{FSB}	$\overline{CS} = V_{CC} \pm 0.2V$ No Address Transitions	C I M			10 15 25		5 8 15	mA
Data Retention Current	I_{CCDR2}	$\overline{CS} = V_{DR}$ min, V_{CC} = 2.0V	C I M					0.5 0.75 6.0	mA
	I_{CCDR3}	$\overline{CS} = V_{DR}$ min, V_{CC} = 3.0V	C I M					1.0 2.0 10.0	
Data Retention Voltage	V_{DR}	V_{CC} input voltage				2.0			V
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.4			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA		2.4		2.4			V

Pin Capacitance (Typical)	Test Conditions	Addresses	Data I/O	$\overline{CS}$, $\overline{WE}$, $\overline{OE}$	Units
	Pin Voltage = 0V, f=1.0 Mhz	8	10	12	pF

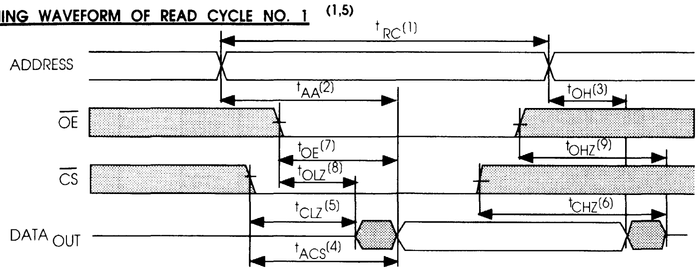
AC Characteristics (1)

No.	S512K8 and S512K8L Parameter	Symbol	45C Min	45C Max	55C,I,M Min	55C,I,M Max	70C,I,M Min	70C,I,M Max
1	Read Cycle Time	t_{RC}	45		55		70	
2	Address Access Time	t_{AA}		45		55		70
3	Output Hold from Address Change	t_{OH}	5		5		5	
4	$\overline{CS}$ Access Time	t_{ACS}		45		55		70
5	$\overline{CS}$ on to Output in Low Z	t_{CLZ} (2,3)	5		5		5	
6	$\overline{CS}$ off to Output in High Z	t_{CHZ} (2,3)	0	20	0	30	0	40
7	$\overline{OE}$ on to Output Valid	t_{OE}		25		30		35
8	$\overline{OE}$ on to Output in Low Z	t_{OLZ} (2,3)	0		0		0	
9	$\overline{OE}$ off to Output in High Z	t_{OHZ} (2,3)	0	20	0	30	0	40
10	Write Cycle Time	t_{WC}	45		55		70	
11	Chip Selection to End of Write	t_{CW}	35		45		55	
12	Address Valid to End of Write	t_{AW}	35		45		55	
13	Address Set-up Time	t_{AS}	0		0		0	
14	Write Pulse Width	t_{WP}	35		45		55	
15	Write Recovery Time	t_{WR}	0		0		0	
16	Data Valid Set-Up to End of Write	t_{DW}	30		35		40	
17	Data Hold from End of Write	t_{DH}	0		0		0	
18	Write Pulse on to Output in High Z	$t_{WHZ(2,3)}$	0	20	0	25	0	30
19	Write Pulse off to Output in Low Z	$t_{WLZ(2,3)}$	5		5		5	
20	Chip Deselect to Data Retention	$t_{CDR(2)}$	0		0		0	
21	Operation Recovery Time	t_R (2)		45		55		70

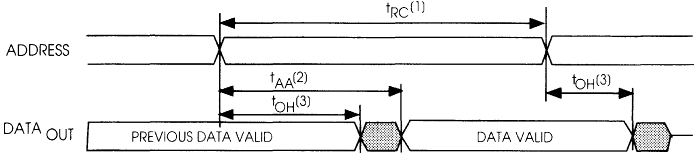
Notes: (1) At Recommended Operating Conditions. All Values in Nanoseconds. (2) This Parameter is characterized initially and after any design or process change which could affect it. It is guaranteed to, but not tested to, the limits specified. (3) All I/O Transitions are measured ± 500mV from steady state with loading as specified in "Load Test Circuits."

READ CYCLE

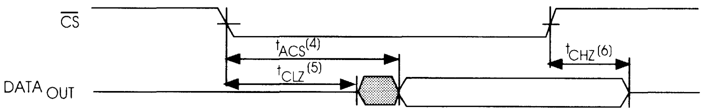
TIMING WAVEFORM OF READ CYCLE NO. 1 [1,5]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1,2,4,5]



TIMING WAVEFORM OF READ CYCLE NO. 3 [1,2,3,5]



Reading the S512K8 device is accomplished by taking chip select (CS) and output enable(OE) LOW, while write enable (WE) remains inactive or high. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/ output pins.

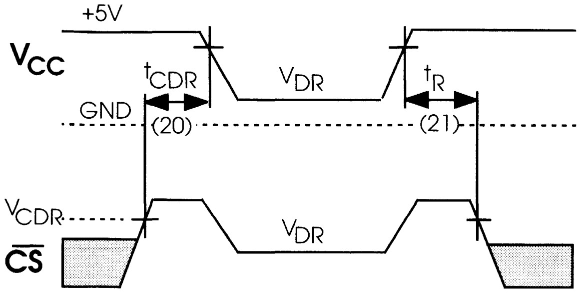
Notes:

1. WE is high for READ CYCLES.
2. Device is continuously selected, CS= V_{IL} for all outputs active.
3. Address valid prior to or coincident with CS transition low.
4. OE =V_{IL}
5. Data Output transitions measured ±500mV from steady state. This parameter is sampled and not 100% tested

Data Retention

S512K8 devices exhibit very low current drain when operated in Data Retention Mode. This Mode is entered by first driving Chip Select to V_{CC} and subsequently driving both V_{CC} and Chip Select to V_{DR}. Chip Select must be set up before the V_{CC} drops below its minimum level. When exiting from Data Retention Mode, the user must wait one full Read Cycle Time prior to asserting Chip Select.

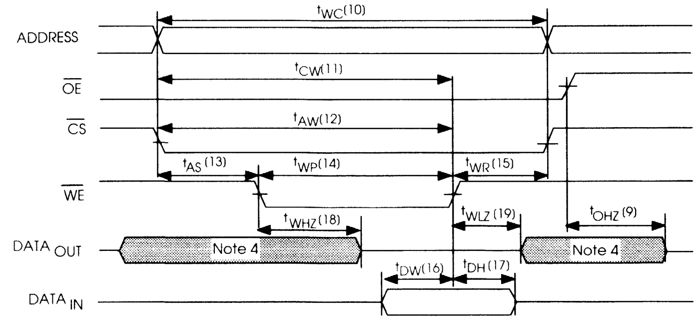
DATA RETENTION TIMING



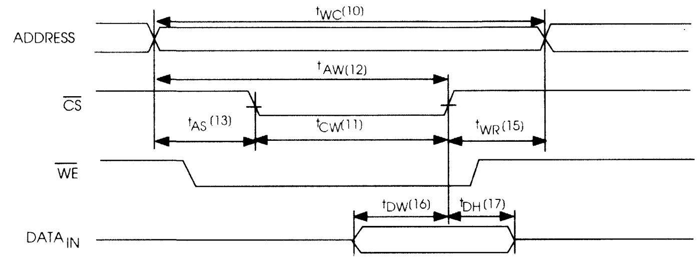
NOTE: V_{CC} +0.2V> V_{CDR} > V_{CC} -0.2V

WRITE CYCLE

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (WE CONTROLLED TIMING) (1,2,3,6,7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CS CONTROLLED TIMING) (1,2,3,5,6)



Writing to the S512K8 is achieved when the chip select (CS) and write enable (WE) inputs are LOW. Data on the input/output pins is written into the memory location specified on the address pins (A0-A18).

The input/output pins remain in a high impedance state when chip select (CS) or output enable (OE) is HIGH, or write enable (WE) is LOW.

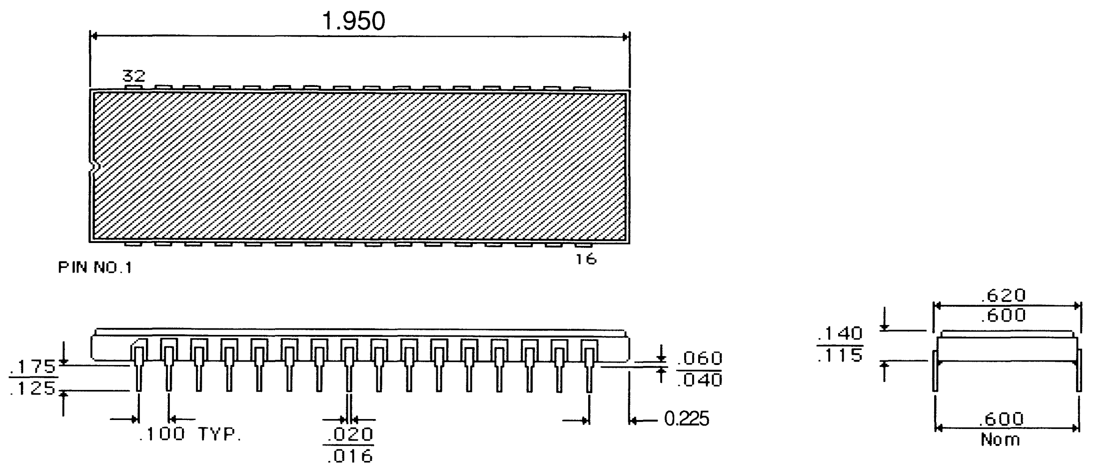
Notes:

1. WE or CS must be high during all address transitions.
2. A write occurs during the overlap (TWP) of a low CS and a low WE.
3. TWR is measured from the earlier of CS or WE going high to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CS low transitions occurs simultaneously with or after the WE low transition, the outputs remain in a high impedance state.
6. Data output transitions are measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
7. During a WE controlled write cycle, write pulse low is ≥TDW + TWHZ to allow the I/O drivers to turn off and data to be placed on the the bus for the required TDW. If OE is high during a WE controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified TWP.

Package Dimension and Ordering Information

32 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
600 MIL WIDE

C



S512K8X-45XX

C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (-40°C to 85°C)
M = Military Temperature Range (-55°C to 125°C)

C = 600 mil Ceramic Sidebrazed DIP

L suffix on base part number = Low Power Device

Printed in U.S.A., AMN-790

Advance Information

256K x 16 Static RAM

Key Parameters **S256K16 and S256K16L**	**Device Types** **55 IC** **55CC**	 **70MC** **70CC** **70CC**	 **85MC** **85IC** **85CC**	 **100MC** **100IC** **100CC**	 **120MC** **120IC**	 **Unit**
Access Time	55	70	85	100	120	nS
Cycle Time	55	70	85	100	120	nS
Output Enable Access	20	25	30	50	50	nS

Features

- **Monolithic 256K x 16 SRAM**
- **Advanced 4-T CMOS technology**
- **48 pin JEDEC standard pinout**
- **Ceramic DIP**
- **Military, industrial, and commercial temperature range**
- **Military grade compliant to MIL-STD-883C**
- **2.0V Low-Power Data Retention Option (S256K16L)**

General Description

The Inova S256K16 is a high performance four megabit Static Random Access Memory (SRAM), organized as 256K sixteen bit bytes.

The S256K16 is manufactured using a highly reliable, four transistor cell CMOS process. This provides a component which combines low active and standby power characteristics with high performance.

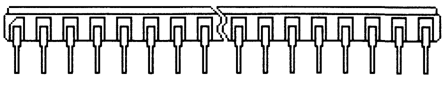
All inputs and outputs are fully TTL compatible. Operation is fully static, so there is no need for extra control logic to generate clocks and timing strobes.

Every military grade device is fully compliant to MIL-STD-883C, paragraph 1.2.1. Industrial and commercial grade devices are produced in the same production line which ensures that they are also of the highest quality.

Pinout/Package Options

1	GND	48	VCC
2	$\overline{\mathrm{OELB}}$	47	I/O0
3	A0	46	I/O1
4	A1	45	I/O2
5	A2	44	I/O3
6	$\overline{\mathrm{WELB}}$	43	$\overline{\mathrm{LB}}$
7	$\overline{\mathrm{CS}}$	42	A3
8	I/O4	41	A4
9	I/O5	40	A5
10	I/O6	39	A6
11	I/O7	38	A7
12	GND	37	A8
13	A9	36	VCC
14	A10	35	I/O8
15	A11	34	I/O9
16	A12	33	I/O10
17	A13	32	I/O11
18	$\overline{\mathrm{WEUB}}$	31	$\overline{\mathrm{UB}}$
19	NC	30	A14
20	I/O12	29	A15
21	I/O13	28	A16
22	I/O14	27	A17
23	I/O15	26	$\overline{\mathrm{OEUB}}$
24	VCC	25	GND

A0-A17	Addresses
I/O 0-15	Data Input/Output
$\overline{\mathrm{CS}}$	Chip Select
$\overline{\mathrm{WEUB}}$	Write Enable Upper Byte
$\overline{\mathrm{WELB}}$	Write Enable Lower Byte
$\overline{\mathrm{OEUB}}$	Output Enable Upper Byte
$\overline{\mathrm{OELB}}$	Output Enable Lower Byte
$\overline{\mathrm{UB}}$	Upper Byte Control
$\overline{\mathrm{LB}}$	Lower Byte Control
VCC	+5 Volt Power
GND	Ground


48 LEAD DIP

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage[1]	V_{CC}	4.5	5.5	V
Input HIGH Voltage	V_{IH}	2.2	V_{CC}+0.5	V
Input LOW Voltage	V_{IL}	-0.5	0.8	V
Operating Temp. Mil.	T_C	-55	125	°C
Operating Temp. Ind.	T_C	-40	85	°C
Operating Temp. Comm.	T_C	0	70	°C

Absolute Maximum Ratings (2)

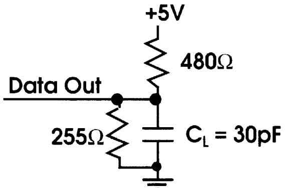
Temperature Under Bias	-55 °C to 125 °C
Storage Temperature	-65 °C to 150 °C
Supply Voltage[1]	-0.5V to 7.0 V
Signal Voltage On Any Pin	-0.5 V to V_{CC} + 0.5V
Power Dissipation	1 Watt
D.C. Continuous Output Current Per Output	20 mA
Lead Temperature (Soldering 10 sec)	260 °C

Notes:

1. All voltages referenced to V_{SS} (GND).

2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Load Test Circuits



C_L = 5pF for t_{CLZ} , t_{CHZ}, t_{BLZ} , t_{BHZ} , t_{OLZ} , t_{OHZ} , t_{WLZ}, t_{WHZ} .

Truth Table

Mode	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OEUB}$ $\overline{OELB}$	$\overline{WEUB}$ $\overline{WELB}$	I/O Operation	Supply Current
Standby	H	X	X	X	X	High Z	I_{SB}
Standby	L	H	H	X	X	High Z	I_{SB}
Standby	≥ V_{CC} - 0.2 V	≥ V_{CC} - 0.2 V	≥ V_{CC} - 0.2 V	X	X	High Z	I_{FSB}
Read	L	L	L	L	H	Data Out	I_{CC2}
Write	L	L	L	X	L	Data In	I_{CC2}

Memory Scale

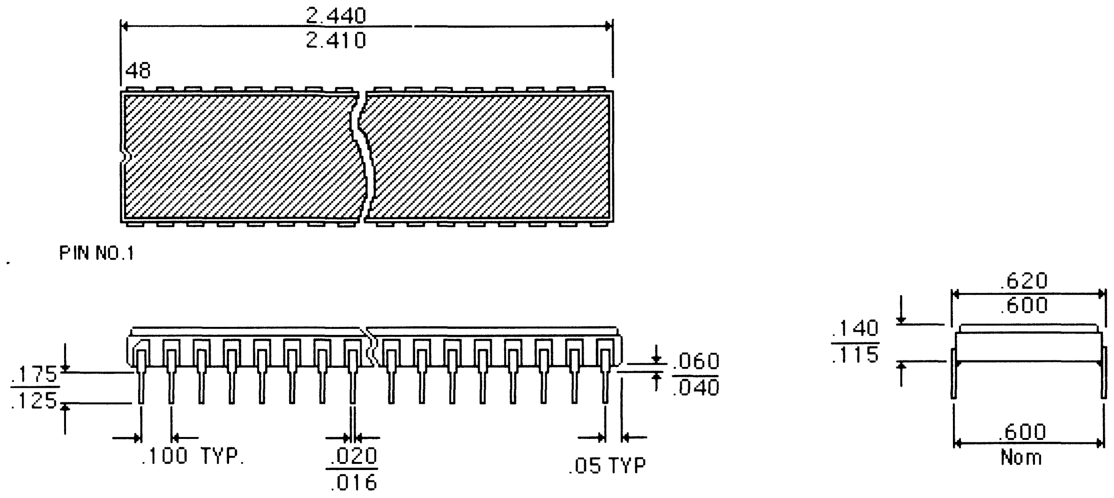
Access Time	55	70	85	100	120	Unit
S256K16	73	57	47	40	33	kbits/ns

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

Package Dimension and Ordering Information

48 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
600 MIL WIDE



S256K16X-45XX

C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (-40°C to 85°C)
M = Military Temperature Range (-55°C to 125°C)

C = 600 mil Ceramic Sidebrazed DIP

L suffix on base part number = Low Power Device

Printed in U.S.A., AMN-790

Advance Information

16K x 32 Cache Memory and Controller

Features

- **Broad Spectrum of Microprocessor Support**
    - **MC68040 Cache Burst Fill, Synchronous Operations to 33.3 MHz**
    - **MC68030 Cache Burst Fill, Synchronous, Asynchronous Operations to 33.3 MHz**
    - **MC68020 Operations to 33.3 MHz**
    - **Byte, Word, Three Byte and Long Word Writes**

- **Flexible Cache Expansion and Mapping**
    - **Integrates Complete Cache Function into a Single Device**
    - **64K Byte Direct Mapping Cache**
    - **Full 32-bit Address Mapping Range**
    - **Multiple Cache Devices Supported**
    - **Maps Four Long Words per Tag Entry**
    - **Maps Four Gigabyte Address Space**

- **Dual Bus Architecture Creates Very High Performance Systems**
    - **C16K32 Placed Between CPU and System Bus Allows Concurrent Operations on Each Bus**
    - **System Bus Performs Independent Block Transfers of Sixteen Long Words**
    - **C16K32 Will Store Four Successive Writes Until System Bus Traffic Clears Up**
    - **Read Byte Word Tracking allows Caching of Byte or Word Devices**

- **Versatile Internal Control Register Configures Cache**
    - **Resettable During Operation or During Power Up**
    - **Sets Synchronous or Asynchronous Operation on CPU Bus**
    - **Permits or Inhibits Caching of References by Function Codes**
    - **Permits or Inhibits System Bus Watching (Snooping)**
    - **Permits or Inhibits Freezing Cache**
    - **Permits or Inhibits System Bus Block Transfers Mode of 4, 8, or 16 Long Words**
    - **Permits or Inhibits Burst Fill Operations from Cache to the CPU**
    - **Permits or Inhibits Write Posting**
    - **Includes Cache Inhibit for System Troubleshooting**

General Description

The Inova C16K32 Cache Memory and Controller is a high performance 64K byte, direct mapping cache memory designed to improve the performance of systems utilizing the Motorola 68000 series of 32-bit microprocessors. The single chip architecture of the C16K32 increases the system performance to a "near zero wait state," and reduces the overall chip count dramatically.

The C16K32 was designed with both performance and versatility in mind. It may be used in the normal three-cycle asynchronous operations of the MC68020 and MC68030, or the faster two-cycle synchronous operations of the MC68030 and MC68040. It services the MC68040 and 68030 CACHE BURST FILL request on a 2-1-1-1 cycle basis if the information is cached. The C16K32 will also allow the CPU direct access to the system bus whenever it receives a CACHE DISABLE, non-cacheable function code, or a reference that is not in the cache when the cache is frozen.

Absolute Maximum Ratings (2)

Temperature Under Bias	0 °C to +70 °C
Storage Temperature	-55 °C to 150 °C
Supply Voltage(1)	-0.3 V to +5.5 V
Input Voltage	-0.5 V to +5.5 V

__Notes__:

1. All voltages referenced to V_{SS} (GND).

2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{CC}= 5.0 VDC+ 5%, GND = 0 VDC, T_A= 0° to 70°C)

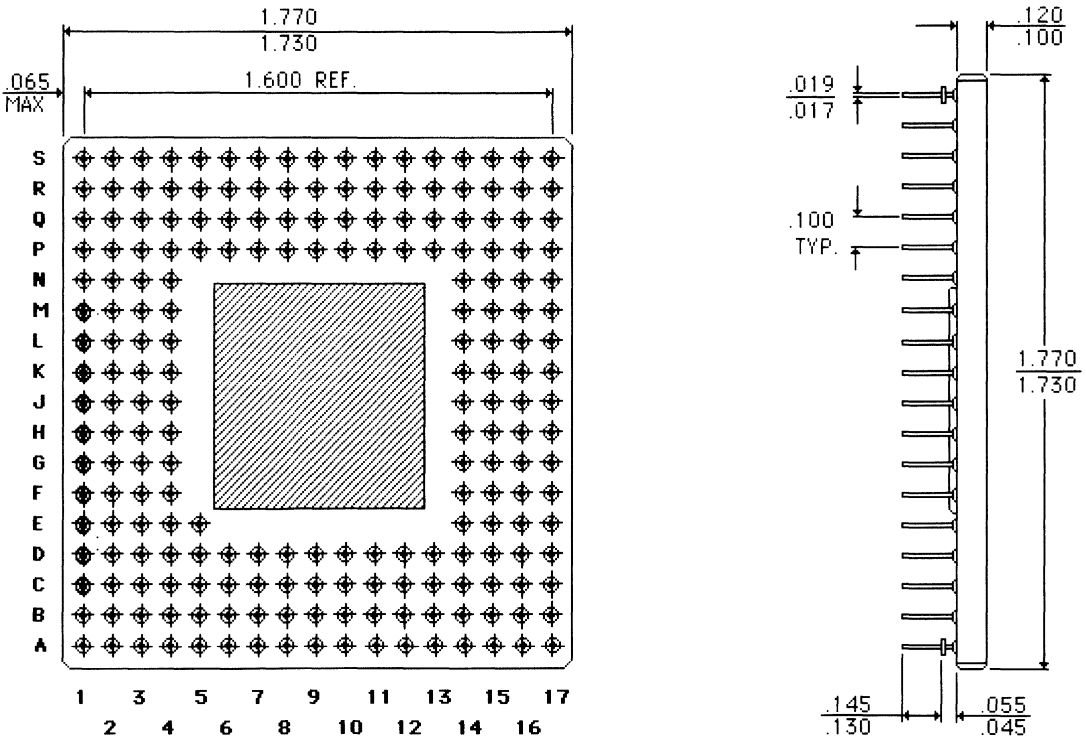
Parameter	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	VCC	V
Input Low Voltage	V_{IL}	-0.5	0.8	V
Input Leakage Current	I_{IN}	-2.5	2.5	µA
High Impedance Leakage Current	I_{TSI}	-20	20	µA
Output High Voltage	V_{OH}	----	2.4	V
Output Low Voltage	V_{OL}	----	0.5	V
Load Capacitance (CPU Bus)	C_{LCPU}		75	pF
Load Capacitance (System Bus)	$C_{LSYSTEM}$		130	pF
except BECS\			50	pF

AC Electrical Specifications - Clock Input

Parameter	Min	Max	Unit
Frequency	DC	33.33	MHz
Cycle Time Clock	30	DC	ns
Clock Pulse Width (1.5V to 1.5V)	14	----	ns
Clock Rise and Fall Times	----	3	ns

Package

209 PIN CERAMIC PIN GRID ARRAY PACKAGE



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Application Notes

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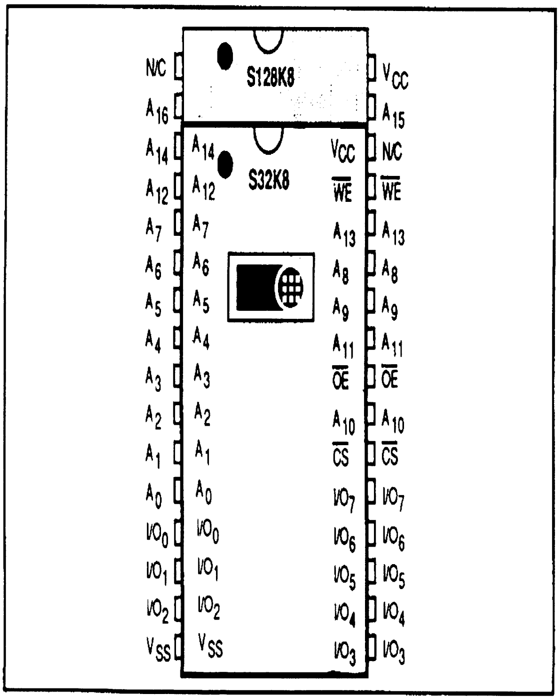
Application Note 1

Upgradeability Assured Using S128K8 Design

Inova has carefully configured the S128K8, its one-megabit, bytewide Static RAM, to provide a smooth upgrade path from 256K bytewide SRAMs to denser memories. By following the simple conventions mentioned below, systems can be designed to use both the S128K8 and lower density, JEDEC-standard 32Kx8 SRAMs in the same 32 pin socket without jumpers. With jumpers, SRAMs up to 512Kx8 can be accommodated.

Package Compatibility: The 28 pin JEDEC DIP and the 32 pin JEDEC DIP pinouts are closely aligned. In fact 27 of 28 pins are a perfect match. Vcc, the 28th, can be connected with one PCB trace connecting Vcc with a "No Connect" at pin 30. This pin becomes the Vcc pin of the smaller package.

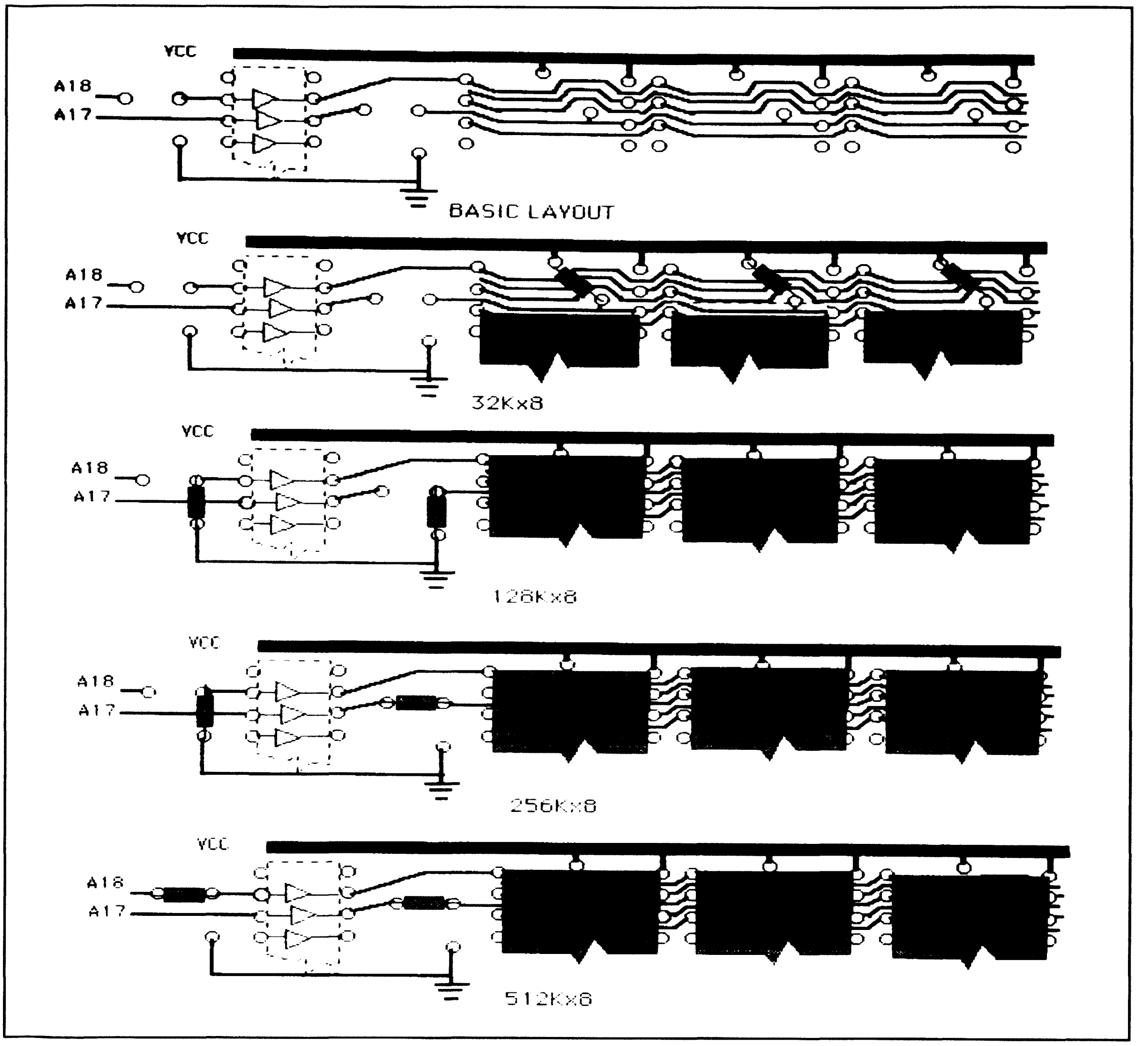


If memory PWB is layed out for the 32 pin S128K8, then any standard 32Kx8 SRAM, including the Inova S32K8 will fit in the lower 28 pins. The only accommodation which need be made is to connect the Vcc pin of the S128K8 (pin 32) to the N/C pin of the S128K8 (pin 30). This trace will supply power for the S32K8 when it is installed and has no effect on the S128K8. This minor change guarantees compatibility between 256K and 1-megabit Bytewide SRAMs.

Future Upgrades: The two N/C pins of the S128K8 are planned for use in two future SRAM products. Pin 30 will be used for Address 17 which is needed on 256Kx8 and 512Kx8 devices. Pin 1 will be used for address 18 required for 512Kx8 devices. These products will be introduced in the 1990s. Knowing this, designers wishing to continue to use the bytewide configurations in future memory assemblies can make their designs compatible with all of these parts.

Pin 1 can be tied across the array and connected to an address driver in present designs. As long as Address 18 is unused by the system, the line can be at any voltage the designer chooses. It is recommended, for array integrity, that the line be driven or jumpered to a level and not allowed to float.

Pin 30 needs to be jumpered to A17 for the 256Kx8 and to Vcc for the 32Kx8. To accomplish this it is suggested that the layout shown on the reverse side should be implemented. Vcc should be run through the array on a heavy bus and connected to pin 32. Local decoupling should be used at each IC. A jumper which may be a piece of wire or a zero ohm resistor should be used to connect Vcc to pin 28 or the S32K8 unit. It should be physically located in the space to be used by the extra pins of the 32 pin memories since it is never used when they are installed. The use of one jumper per memory device is suggested so that the Vcc pin is electrically close to a decoupling capacitor. Pin 30 should also be connected across the array in a manner similar to Pin 1, however, a jumper should also be connected across the array in a manner similar to Pin 1, however, a jumper should be installed between the array pins and the driver pin so that it can be removed when the S32K8 is installed, isolating the driver output from Vcc.



BASIC LAYOUT

32Kx8

128Kx8

256Kx8

512Kx8

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Application Note 2

USING MEMORY MODULES AS SECOND SOURCES

Overview

The S128K8, manufactured by INOVA Microelectronics, is a 1 Megabit, monolithic, CMOS Static RAM. It can be second sourced by modules which are available from a number of sources.

Modules are functional replacements of the S128K8, but they exhibit *significantly higher pin capacitances.* These high capacitances slow down address and data transitions at the board level. The slow down increases in direct proportion to the number of modules in the memory array. This, in turn, means that in many systems the access time specification of the module used to second source the S128K8 must be faster than the S128K8 in order to work in the same socket.

A second difference which some designers may wish to consider is reliability. Due to the increased component count, modules are less reliable than monolithic parts. In addition to their natural reduction in reliability, their higher capacitance results in more power being dissipated in the drivers. This higher power may reduce the reliability of these drivers, as well.

This Application Note explores these characteristics and provides methods of evaluating the differences between modules and S128K8s for various types of drivers.

Specification Comparison

Modules are socket compatible subsystems which can be used as devices. They consist of a substrate with 32 pins attached in a configuration similar to a true JEDEC standard DIP. On this substrate, module manufacturers attach four 256K LCC static RAMs along with a decoder and capacitor to build up the equivalent of a one megabit device.

Below is a tabular comparison of four different 128K8 modules and the S128K8 monolithic device. Of course the modules have higher capacitance specifications. The I/O test column represents the load volume which each manufacturer uses in his test. This load is used to simulate board and device capacitance found in normal system usage.

A second specification of interest in this study is the Output drive capability. These specifications are listed in Table 1B.

Table 1A. Capacitance Specifications (pF)

Vendor	P/N	I/O	Address	Clock	I/O Test
Mosaic	MS8128SC	35	27	6	100
EDI	EDI8M8128C	43	50	10	100
IDT	IDT8M824S	40	35	—	30
Hitachi	HM66204	50	45	—	100
Inova	**S128K8**	**8**	**5**	**5**	**30**

Table 1B. Output Specifications

Vendor	P/N	V_{OH}(V) @	I_{OH}(mA)	V_{OL}(V) @	I_{OL}(mA)
Mosaic	MS8128SC	2.4	-1	0.4	2.1
EDI	EDI8M8128C	2.4	-1	0.4	2.1
IDT	IDT8M824S	2.4	-4	0.4	8.0
Hitachi	HM66204	2.4	-1	0.4	2.1
Inova	**S128K8**	**2.4**	**-4**	**0.4**	**4.0**

Output Characteristics

When a device is required to drive a capacitor it slows down proportionally to the size of the capacitor. For some loads this slow down is negligible and most designers can ignore it. When using Modules, the I/O capacitance may be high enough that it enters into the access time equation.

It is straightforward to calculate tha access time pushout due to capacitive loading. First one should know the output characterisitics of the device. The manufacturer should be able to supply this, although it is not always included in data sheets.

Figure 1 and 2 show the Output Characteristics of the S128K8. The dotted lines represent straight line approximations of the characteristics. Using straight line approximations greatly simplifies the math involved in the calculations and eliminates curve fitting exercises.

The two equations of the characteristic are also very simple. These are from V_{OL} = 5.0V to 2.5V,

$$I_{OL} = .06A,$$

and from V_{OL} = 2.5V to OV,

$$I_{OL} = .024 \times V_{OL}$$

To calculate the time to move the output from one to zero (5V - 0.8V), two separate times are calculated. First the time from 5V to 2.5V, then from 2.5V to 0.8V.

The first is a simple equation:

$$t_1 = C \bullet \Delta v / i = 41.67C$$

To determine the second, a common integration is necessary.

$$\int_{t_1}^{t_2} d_t = -C \int_{2.5}^{0.8} \frac{dv}{.024V_{OL}} \text{ so that,}$$

$$t_2 = t_1 + 41.67C\,(1n\,0.8 + 1n\,2.5)$$

$$t_2 = 89.14C$$

The derivation of a similar equation can be performed for driving from zero to one. The voltages are 0 to 2.4V and are part of the constant curve only.

$$t_{OH} = C \bullet \Delta v / i$$

$$t_{OH} = 52.17C$$

Figure 1. V_{OL}/I_{OL} S128K8

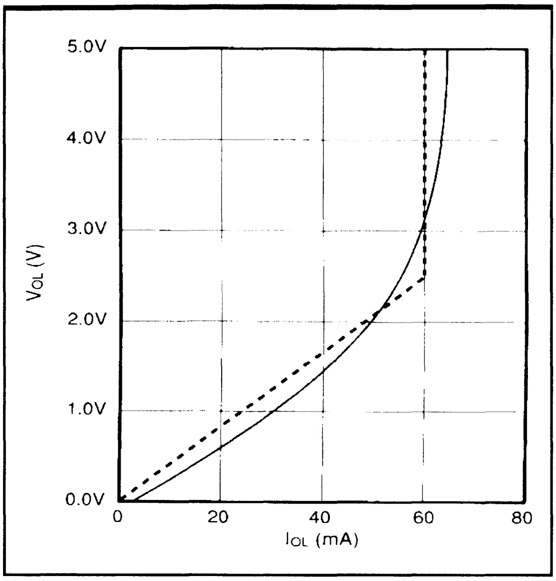


Figure 2. V_{OH}/I_{OH} S128K8

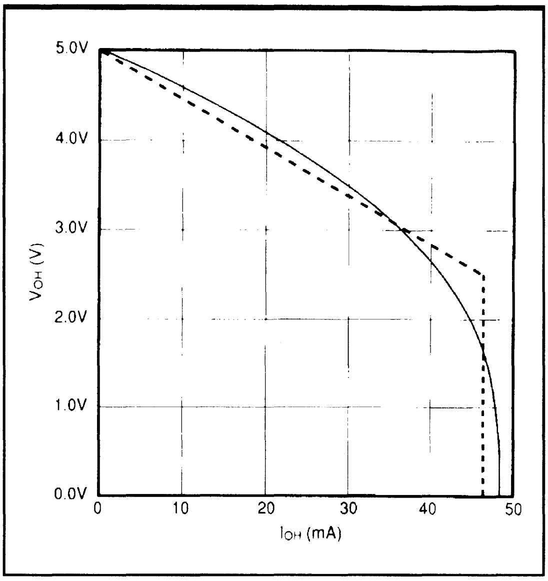


Table 2. S128K8 Loading Pushout (nS)

Load Description	C(pF)	t_F(nS)	t_R(nS)	Pushout (nS)
One Device + Test	38	3.39	1.99	
One Device	8	0.71	0.42	-2.67
Two Devices	16	1.43	0.84	-1.96
Four Devices	32	2,85	1.68	-0.53
Eight Devices	64	5.7	3.36	2.32

The effect of capacitance on the access time of the S128K8 can now be calculated. First we calculate the rise and fall times with one output and a test load. Then we calculate the rise and fall times with one, two, four and eight loads and subtract the rise and fall time of the test condition. This provides a number which we call "loading pushout."

The S128K8 has been tested with a load which provides margin for up to four devices on the I/O line. With eight devices on an I/O line a designer should expect that 2.3 nanoseconds of extra access time (as shown in Table 2) should be planned into the system design.

The same analysis can be performed for each of the modules listed in Table 1. Of course with modules the capacitance is higher which, in turn, increases the severity of this problem.

The analysis of each module is performed in Appendix A but is presented here in graphical form. The range of module pushout times is plotted as a group and the S128K8 pushouts are compared to these.

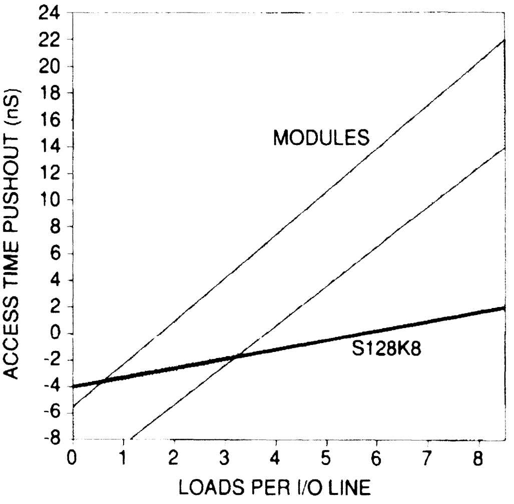
When only one or two devices are on an I/O line, both modules and S128K8 should perform faster than specification due to the fact that they are tested with higher loads than they see in this situation.

Due to their larger loading factors, modules quickly grow worse than specified. By the time four loads are on the I/O line, an average of 4 nanoseconds should be added to access time to cover the modules, while the S128K8 is still faster than tested.

It is uncommon to see I/O lines longer than eight devices. This, after all, represents a memory with 1024K words of data. Some boards for very large memories may be required to have longer lines. If this is the case the designer needs to look at this aspect very carefully and be sure to account for the lost access time due to the I/O capacitance.

The higher the capacitance the longer it will take to switch. The second variable is the driver. Different types of circuits will produce different amounts of current, and thus have different switching times.

Figure 3. I/O Pushout Comparison S128K8 vs. Modules



Input Capacitance

It is more likely that address access time will be pushed out for three reasons. First, the capacitance is nearly as high as the I/O capacitance. Second, the inputs are not pre-loaded in test to provide system margin. And third, the opportunity to connect more devices in parallel exists since arrays are two dimensional and the I/O lines are only one dimensional.

The time required to switch the inputs will have two variables. First, of course, is the input itself.

We have analyzed the problem using three types of drivers: HCMOS, LSTTL and FAST logic. Each memory designer may have to perform this task using board specific drivers and arrays. We have relegated the specifics to Appendix B for reference but have treated the analysis in the same manner as we did the I/O derivations in the previous section.

The inputs are virtually 100% capacitive on both the S128K8 and the modules. Input leakage is specified between two and fifteen microamps on all devices. This means that drivers driving these loads will be at their "No-Load" output voltage when the system is at rest. The load capacitor will have to be driven from this voltage to the switching voltage of the load device. For both the S128K8 and modules this is 1.5V since that is the voltage from which all measurements are initially made in final test.

Table 3 shows the result of the analysis of various drivers in terms of the load capacitance. Each driver switching speed can be stated as a constant multiplier of the load capacitance it sees. This serves as an excellent tool to evaluate the drivers and the speed of the system.

To derive the actual switching time using Table 3, simply substitute the actual load value for C. If C were 100 pF, HCMOS drivers would switch from high to low in 11.7 nanoseconds. Since no two input capacitance specifications are the same, however, each vendor's parts will switch at different times for the same number of devices.

The reader is cautioned that the "actual" load value is affected by many variables and is difficult to predict. Because of this, these calculations should be used as guidelines rather than exact results.

These numbers can serve as a design guide to speed up the system. For instance, if a designer is using HCMOS, it may be advisable to add a gate to assure that the critical transition is always made from low to high if the load capacitance is large. While this would slow down the start of the transition, it would complete the transition almost three times faster. In large arrays this may be important.

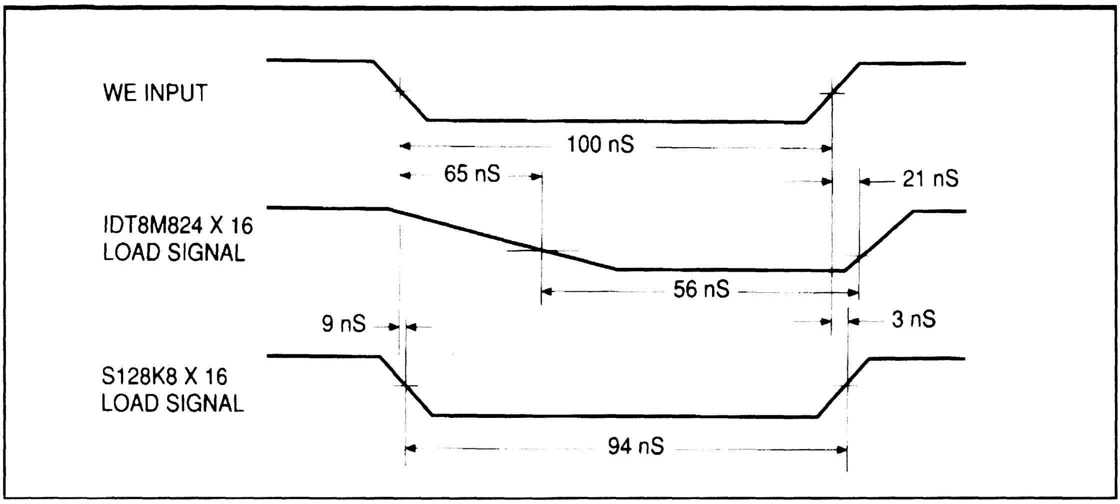
The transition speeds are significant for two interrelated reasons. The first is timing relationship skews. The capacitance in large arrays affects rise and fall time differently. HCMOS fall times are three times as long as rise times. If an array of 16 modules is driven with HCMOS and uses a common write enable, one could expect the $\overline{\text{WE}}$ in the array to be narrower than the formed pulse on the board as illustrated in Figure 4. A load of 16 S128K8s is shown using the same driver.

This simple analysis is illustrative of the effects of varying capacitance in memory arrays. The designer must approach the problem carefully because the ability to mix and match components

Table 3. Driver Family Switching Times vs. Capacitive Load

	To drive the Load C from			**To drive the Load C from**		
Driver Type	**V_{OH}(nl) of Driver(V)**	**ToV_{SW} of Load(V)**	**Takes (nS)**	**V_{OL}(nl) of Driver(V)**	**To V_{SW} of Load (V)**	**Takes (nS)**
HCMOS	5.0	1.5	117.0C	0.0	1.5	38.0C
LSTTL	4.4	1.5	12.9C	0.3	1.5	24.0C
FAST	3.8	1.5	10.2C	0.3	1.5	12.2C

Figure 4. Timing Skews Driving Capacitive Memory Arrays Using HCMOS Drivers



properly is important to most system assemblers.

The second reason that transition speed is significant is that access time deteriorates due to it. Memory devices are graded by speed. Faster devices cost more than slower ones. Long transition times mean faster devices must be used to crate an equivalent memory. This increases the system memory cost.

The access time of memories, assuming that all other signals are properly timed, is a result of both the input capacitance transitions and the I/O pushout mentioned earlier.

To calculate the total access time of a memory system, one needs to add the transition time to the pushout time. For average memories such as a 512Kx32 bit design, one would need to add the I/O loading pushout for four devices to the switching time for a 4x4 array (16 devices). If 74LS244 were the driver and S128K8 were the device, the following calculation would provide the system access time which would need to be added to the normal logic delays

I/O Loading Pushout	-0.53
Address Switching	5.6
TOTAL	5.07 nS

If we were to compare this to MS8128SC we would find the following:

I/O Loading pushout	0.45
Address Switching	21.1
TOTAL	21.55 nS

To observe a worst case situation we will look at a 1024Kx32 bit array driven with two sets of 74LS44 drivers. Each set of drivers will drive 16 loads and each I/O line will see eight devices. We will compare all of the devices under the conditions outlined in Table 4. See Appendices A and B for details of the calculations.

As we see in Table 4, there may be substantial access time penalty paid for the use of modules as second sources. The best a designer can do is to be aware of these differences and take appropriate actions to ameliorate them. This can be done by splitting the loading between drivers, splitting the I/O lines, or buying modules at a faster speed than the S128K8.

Of these options the most desirable is to split the address loading since this is least expensive and easiest in layout. Splitting the I/O involves eight lines per device so this may result in layout problems depending on the strategy involved. Buying modules at a specification which accounts for the difference requires buying faster parts and results in a more expensive solution.

Power

A result of high input capacitance, which is not well recognized, is the increase in power required to drive the array. Depending on the size of the array this can be significant.

The power required to drive the array depends to some extent on how it is designed and operated. A common method in building a 512K x 32 bit array would be to select each row with a separate $\overline{\text{CS}}$ and provide a global $\overline{\text{WE}}$ or $\overline{\text{OE}}$. Addresses would be driven globally. Since $\overline{\text{CS}}$ is decoded and only one row is on at any time, a user might believe that this is a low power design. In fact if any analysis is done based on the data sheet specifications for device current, one would arrive at Table 5.

If this array is run at 100 nS cycle time through all addresses, we can calculate the power required to operate it. Assume that addresses change once per cycle and clocks change twice per cycle. Further, assume that only half of the addresses change at one time (binary distribution) and that one clock ($\overline{\text{WE}}$ or $\overline{\text{OE}}$) changes to all devices while one clock ($\overline{\text{CS}}$) changes to four devices. All of these assumptions will be true in the 512K x 32 bit array discussed above.

The governing equation is,

$$\text{Capacitive Power} = C \times V2 \times f$$

C is the input capacitance times the number of inputs driven. V is the voltage through which they are driven and for the driver in question is V_{OH} (nl) - V_{OL} (nl); f is the frequency.

Addresses which change an average of one time per cycle have a period of two cycles or 200 nS. If there are 17 addresses to 64 devices and an average of 50% of these change at any one time, the number of driven inputs would be 17 x 16 x .5 = 136 at 200 nS. Clock inputs would add a small number to this. There is one clock ($\overline{\text{OE}}$ or $\overline{\text{WE}}$) to

Table 4. Variations on Access Time Due to Module Loading. 1024K x 32 Array ; 74LS244 Drivers

	S128K8	MS8128SC	EDI8M8128	IDT8M824	HM66204
I/O Loading Pushout (nS)	2.32	12.93	17.92	22.29	22.24
Address Switching (nS)	3.84	20.74	38.40	26.88	34.56
Totals (nS)	**6.16**	**33.67**	**56.32**	**49.17**	**56.84**
Module Access Penalty (nS)		27.51	50.16	43.01	59.64

16 devices at 100 nS. The $\overline{CS}$ clock is much lower capacitance and goes to only four devices at a time so we can ignore its influence.

Table 6 shows the increase in current due to the capacitive inputs of the array. Two significant features should be pointed out. The first is the obvious increase in current due to higher levels of capacitance. Current requirements for S128K8 are increased only 1.5% while for modules the increase is an average 15% over expected current.

Under worst case conditions the instantaneous power may be even higher. If we assume that all addresses switch every cycle the switching current would almost double. While it would probably not be very useful to constantly access only two memory locations (Address-Address Complement) the system should certainly be able to do it.

The capacitive power causes another problem which is less obvious. The dissipation of the power to the array occurs in the drivers. If eight of the 18 total lines are contained in one package such as a 74F244, then 44% of the switching power will be dissipated in the package. this could increase average driver package power by over 300 mW and the instantaneous power could climb even more. Designers should pay close attention to this when driving large arrays. The increase in power may cause a long term degradation in the reliability of the array drivers.

Table 5. Specified Current Requirements for a 512Kx32 Memory Array

Device	**Active current (mA)**	**+**	**Standby Current (mA)**	**=**	**Total (mA)**
S128K8	**110 x 4 = 440**		**40 x 12 = 480**		**920**
MS8128SC	100 x 4 =400		18 x 12 = 216		616
EDI8M8128C	95 x 4 = 380		50 x 12 = 600		980
IDT8M824S	160 x 4 = 640		15 x 12 = 180		820
HM66204	80 x 4 = 320		12 x 12 = 144		464

Table 6. Actual Current Requirements for a 512K x 32 Memory Array

Device	**Input (pF)**	**Capacitive Power (mW)**	**Switching Current (mA)**	**^{I}CC (mA)**	**^{I}TOTAL (mA)**
S128K8	**5**	**69.8**	**14**	**920**	**934**
MS8128SC	27	376.7	75	616	691
EDI8M8128C	50	697.6	139.5	980	1119.5
IDT8M824S	35	488.3	97.7	820	917.7
HM66204	45	627.8	125.5	464	589.5

Reliability

The reliability of a device can only be measured after it is built. Usually many devices are operated for many hours to determine this number. Actual device reliability is a measure of both the design and the care and constancy of the operation which built it.

In an effort to predict device and system reliability, the Department of Defense publishes MIL-HDBK-217E. This publication describes methods of calculating "predicted reliability" of parts which may not even have been designed. These predictions allow designers to investigate various designs prior to implementation so that they can estimate the probability of mission success under varying conditions.

We have used this tool to evaluate the differences between modules and S128K8s. Appendix C is devoted to the actual calculation and should be reviewed only by those readers who have the intestinal fortitude for long boring calculations involving the summation of a lot of small numbers.

Equivalent conditions were used for both types of device and it was found that the S128K8 would have a failure rate of 3.605 failures per million hours and the failure rate for modules would be 7,537 failures per million hours.

It should surprise no one that the reliability of a 1-megabit part is better than the reliability of four 256 Kilobit parts. The truth of the matter is that the modules are all subassemblies and must be treated as miniature printed circuit assemblies rather than integrated circuits.

This decrease in predicted reliability will affect system reliability in direct proportion to the percentage of the system which is memory. If there are only one or two parts per system the effect will probably not be noticed. If, however, there is a high percentage of memory in the system, the designer should approach the use of modules with caution.

Conclusions

Modules have seven to ten times the pin capacitance of monolithic parts. Nevertheless, they can be used as second sources for S128K8 provided the following principles are kept in mind.

- High I/O capacitances exhibited in arrays of modules can result in access time pushout relative to their own specification.
- High input capacitance slows down the address and clock drivers to memory module arrays, further slowing access times.
- The high capacitance causes greater power dissipation in both the array and its drivers.
- System memory reliability will be reduced whenever modules are used in place of the S128K8.
- All of the above effects increase in severity in direct proportion to the number of modules in the array.

System designers should carefully review their use of modules. The high input capacitance of modules will slow down system access, alter expected timing, and increase skews.

On the other hand, S128K8 can be used to replace modules with no degradation to system access time and with an improvement in reliability.

When replacing modules with S128K8s the designer should carefully review the system specifications. It is often possible to use slower S128K8s than the module device previously used in the system. This ability to use slower parts means that they will be more cost effective.

Appendix A

Output characteristics for modules are not regularly published in data sheets. The analysis of module access time pushout was performed using the S128K8 output characteristic. Since all the modules listed have CMOS outputs and each in turn have similar or lower specified drive capability than the S128K8, the assumption of similar output characteristics should provide a comparison favorable to modules.

An analysis similar to the one for the S128K8 in the body of the text was performed for each of the modules. The results are shown in the following tables.

Table A1. MS8128SC Loading Pushout

Load Description	**C(pF)**	**t_F(nS)**	**t_R(nS)**	**I/O pushout (nS)**
One device + test	135	12.03	7.08	
One device	35	3.12	1.84	-8.91
Two devices	70	6.24	3.67	-5.79
Four devices	140	12.48	7.35	0.45
Eight devices	280	24.96	14.69	12.93

Table A2. ED18M8128C Loading Pushout

Load Description	**C(pF)**	**t_F(nS)**	**t_R(nS)**	**I/O pushout (nS)**
One device + test	143	12.75	7.50	
One device	43	3.83	2.26	-8.91
Two devices	86	7.67	4.51	-5.08
Four devices	172	15.33	9.02	2.59
Eight devices	344	30.66	18.05	17.92

Table A3. IDT8M824S Loading Pushout

Load Description	**C(pF)**	**t_F(nS)**	**t_R(nS)**	**I/O Pushout (nS)**
One device + test	70	6.24	3.67	
One device	40	3.57	2.10	-2.67
Two devices	80	7.13	4.20	0.89
Four devices	160	14.26	8.40	8.02
Eight devices	320	28.52	16.79	22.29

Table A4. HM66204 Loading Pushout

Load Description	C(pF)	t_F(nS)	t_R(nS)	I/O Pushout (nS)
One device + test	150	13.37	7.87	
One device	50	4.46	2.62	-8.91
Two devices	100	8.91	5.25	-4.46
Four devices	200	17.83	10.49	4.46
Eight devices	400	35.66	20.98	22.24

Appendix B

To understand the overall effect of input capacitance, we must begin by determining the output characteristic of the load driver. The first quality which we must know is the No Load output voltages of the driver type selected. This investigation will review three different driver types: HCMOS, FAST and LSTTL. In Table B1 a list of the No Load Output Voltages for these devices is given.

It is important to know these voltages to establish the proper drive equation. When a system is at rest, these will be the levels of the output drivers. When switching the capacitor from a low to a high the speed of the transition must be measured from V_{OL} (nl) to 1.5V. When switching from a high to a low the transition must be measured from V_{OH} (nl) to 1.5V. All transitions are measured to 1.5V.

Table B1. No Load Outputs of Drivers

	$V_{OH\,(nl)}$	$V_{OL\,(nl)}$
HCMOS	5.0	0.0
FAST	3.8	0.3
LSTTL	4.4	0.3

Next we must know the V_{OH}/I_{OH} and V_{OL}/I_{OL} characteristics of the drivers. Once we understand these characteristics, a simple calculation can be performed to derive a switching time as a function of capacitance for each type of driver and load.

To begin with we will study HCMOS characteristics shown below. These devices are frequently used for lowest power. We can closely approximate the curve with a couple of straight lines. These are shown as dotted lines in Figure B1.

From these curves we can derive two equations for each set of straight lines.

From V_{OL} = 5V to 1.5V,

$$I_{OL} = 0.0017V_{OL} + 0.24$$

and from V_{OL} = 1.5V to 0V,

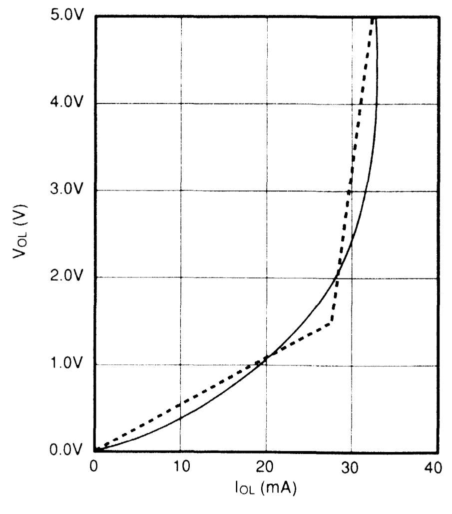
$$I_{OL} = 0.018V_{OL}$$

In this instance, we need only calculate t1 across the entire range of I. Since this is the end point of the curve, no further calculations are required.

$$\int_{0}^{t_1} dt = C\int_{5}^{1.5} \frac{dV_{OL}}{0.0017V_{OL} - .024}$$

$$t_1 = 117C$$

Figure B1. V_{OL} / I_{OL}, HCMOS Driver



To drive the inputs high the V_{OH}/I_{OH} characteristic, shown in Figure B2, is used. The equations are:

From $V_{OH} = 0V$ to 2.5V,

$I_{OH} = 0.002V_{OH} - 0.041$

and from $V_{OH} = 2.5V$ to 5V,

$I_{OH} = 0.0144V_{OH} - 0.072$

To determine the switching speed in the low direction only the first equation need be used. A simple integration over the required boundaries provides the result.

$$\int_{0}^{t} dt = C\int_{0}^{1.5} \frac{dV_{OH}}{0.002V_{OH} - 0.041}$$

t = 38C

Low power Schottky drivers are used when speed is needed but low noise signals are considered critical. The output characteristics are shown in Figure B3 and B4.

The characteristic can be analyzed using the same procedure as above:

For $V_{OH} = 0V$ to 3.0V,

$I_{OH} = 0.016V_{OH} - 0.065,$

which covers the entire range of interest. Then

$$\int_{0}^{t} dt = C\int_{0.3}^{1.5} \frac{dV_{O}}{0.016V_{OH} - 0.065}$$

and

t = 24C

Figure B2. V_{OH} / I_{OH}, **HCMOS Drivers**

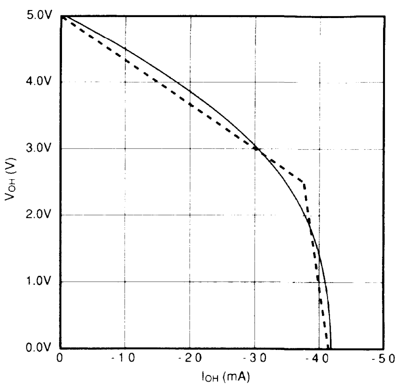
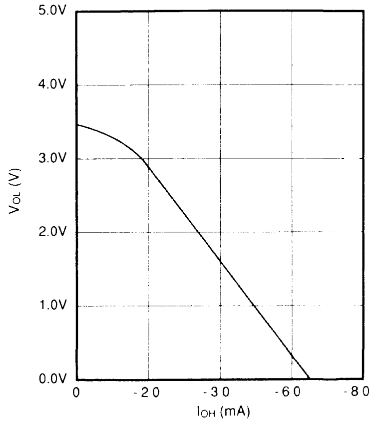


Figure B3. V_{OH} / I_{OH}, **LSTTL Drivers**



In this instance only the lower 0.4V of the curves is shown in Figure B4. We can project a curve from that

$$I_{OL} = 0.175V_{OL} - 0.04$$

Since we know that the curve has a cutoff at I_{OS}, we could use that number for I to determine the voltage over which this is accurate.

$$0.225 = 0.175V_{OL} - 0.04 \text{ and}$$

$$V_{OL} = 1.5V$$

If we use this as the breakpoint we find that from V_{OH} (nl) to 1.5V

$$I = .225A$$

which covers the range of interest.

The switching time is therefore:

$$t = C\,(4.4 - 1.5)/.225 = 12.9C$$

The next set of characteristics to analyze would be FAST Logic. Specific characteristics will be for 74F244 Quad Buffers. These parts are commonly used when speed is of critical importance to the design.

The only equation of interest for the V_{OH}/I_{OH} characteristic is the straight line from 3.25V to 0V. The equation is

$$I_{OH} = 0.13 - 0.033V_{OH}$$

setting this into the equation for switching speed yields:

$$\int_{0}^{t} dt = C\int_{0.3}^{1.5} \frac{dV_{OH}}{0.13 - 0.033V_{OH}}$$

so that,

$$t = 12.2C$$

Figure B4. V_{OL} / I_{OL}, LSTTL Drivers

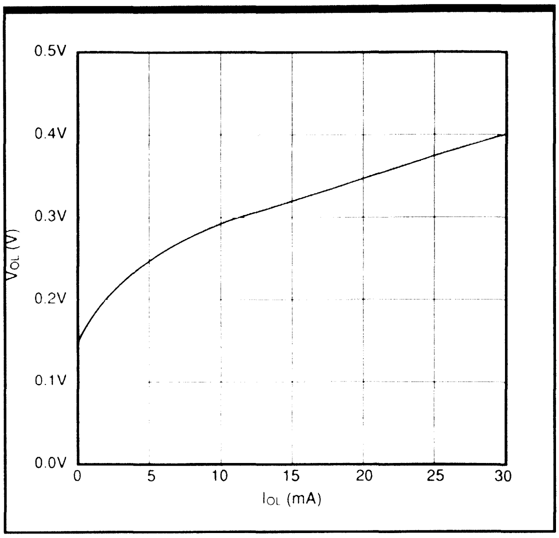
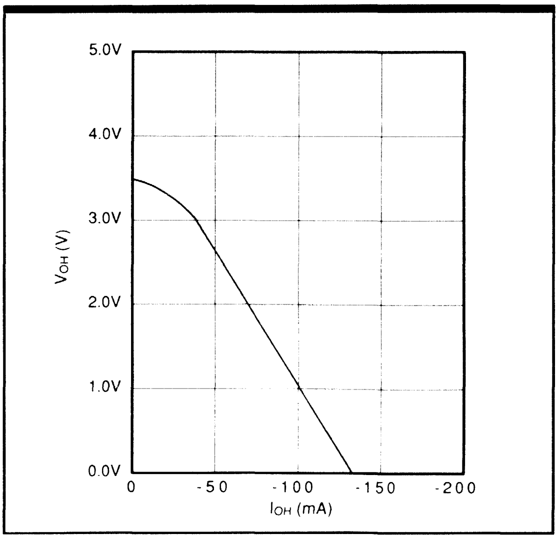


Figure B5. V_{OH} / I_{OH}, FASTDrivers



For the V_{OL}/I_{OL} characteristic, there are two interesting sections of the curve. The characteristic has a specific slope until current limiting at Ios occurs. Then it is limited to 0.225 A.

The characteristic can be approximated with two lines represented by two equations:

From $V_{OH}(nl)$ to 0.9V,

$I_{OL} = .225$

and from 0.9V to 0.225V,

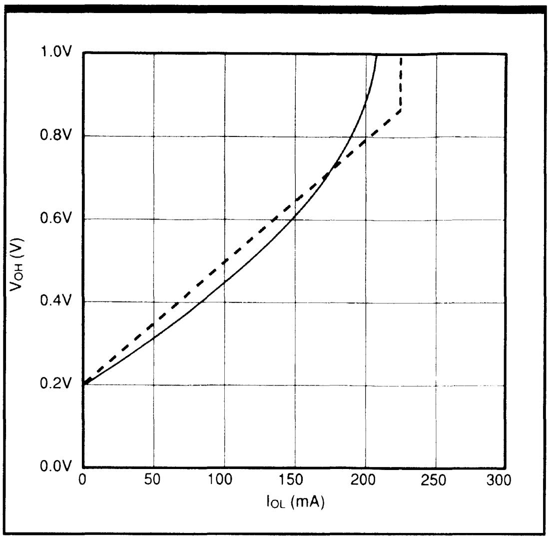
$I_{OL} = 0.346\ V_{OH} - 0.087$

Only the first equation is relevant and,

$t = C\ (3.8 - 1.5)/.225$

$t = 10.2C$

Figure B6. V_{OL}/ I_{OL}, FAST Drivers



Appendix C

This analysis uses the formula in MIL-HDBK-217E to determine the differences in device reliability. A more complete explanation for each formula is found in the MIL-HDBK-217kE and it is suggested that the reader familiarize himself with these methods.

A ground based fixed environment is assumed for all equipment. This leads to other assumptions. First the actual case temperatures of both devices will be 45°C and the junction temperatures are 75°C.

For the S128K8, the base equation for CMOS Static RAM failure rate per million hours is shown as:

Table C1. S128K8 Predicted Reliability

Formula	**MIL-HDBK-217E Reference**
$\lambda_P = \pi_Q * \pi_L * (C_1 * \pi_T * \pi_V + C_2 * \pi_E)$	5.1.2.4
where	
$\pi_Q = 2$ for the quality factor B-1	5.1.2.7-1
$\pi_L = 1$ for a mature device	5.1.2.7-2
$\pi_T = 2.2$ for $T_J = 75°C$	5.1.2.7-8
$\pi_V = 1$ for $V_{DD} < 12V$	5.1.2.7-14
$\pi_E = 2.5$ for ground based fixed equipment	5.1.2.7-3
$C_1 = 0.8$, circuit complexity for 1 Mb (est)	5.1.2.4
$C_2 = 0.017$, package complexity factor	5.1.2.7-16
and so	
$\lambda_P = 2 * [0.8 * 2.2 + 0.017 * 2.5] =$ **3.605 failures/million hours**	

For a module we have exactly four 256K byte-wide CMOS SRAMs and a decoder and capacitor all surface mounted on a ceramic substrate. The capacitor is used as a decoupler. Since a failure of the capacitor may not cause circuit failure, the effect of this has been ignored.

A detailed formula for module reliability has not been proposed in MIL-HDBK 217E so it will be treated as a printed circuit assembly.

Three factors change. First, there are now four memories with better individual reliability but worse combined reliability. Second, there is a decoder which must be included in the calculations and third, the interconnections of the substrate must now be included. Each of these will be calculated individually and the sum of them will be the device reliability. For the 256K CMOS SRAMs packaged in LCC we have:

Table C2. 256K LCC Predicted Reliability

Formula	**MIL-HDBK-217E Reference**
$\lambda_P = \pi_Q * \pi_L * (C_1 * \pi_T * \pi_V + C_2 * \pi_E)$	5.1.2.4
where	
$\pi_Q = 2$ for the quality factor B-1	5.1.2.7-1
$\pi_L = 1$ for a mature device	5.1.2.7-2
$\pi_T = 2.2$ for $T_J = 75°C$	5.1.2.7-8
$\pi_V = 1$ for $V_{DD} < 12V$	5.1.2.7-14
$\pi_E = 2.5$ for ground based fixed equipment	5.1.2.7-3
$C_1 = 0.4$, circuit complexity for 256K	5.1.2.4
$C_2 = 0.01$,for 28 active pins of an LCC	5.1.2.7-16
and so	
$\lambda_P = 2 * [0.84* 2.2 + 0.01 * 2.5] =$ **1.81 failures/million hours**	

For the CMOS Decoder packaged in LCC for which nine pins are active we have the same number as shown in Table C2 with the following exceptions.

Table C3. CMOS Decoder Predicted Reliability

Formula	**MIL-HDBK-217E Reference**
$C_1 = 0.06$, circuit complexity for <100 gates	5.1.2.1
$C_2 = 0.003$, for 9 active pins of an LCC	5.1.2.7-16
and so	
$\lambda_P = 2 * [0.06* 2.2 + 0.003 * 2.5] =$ **.279 failures/million hours**	

The interconnections on the substrate are assumed to be complete without plated through holes. All LCC's are connected by reflowing solder. Each memory IC has 28 active connections and the decoder has nine. the formula for a reflow solder PCB is:

Table C4. Substrate Predicted Reliability

Formula	**MIL-HDBK-217E Reference**
$\lambda_P = \pi_E * N_1 * l_{Bi} * \pi_{Ti} * \pi_{Qi}$	5.1.14
where,	
$\pi_E = 2.1$ an environmental factor dertimined in	5.1.14-2
$N_i = 121$ which is the number of connections	
$\lambda_B i = 0.000069$ for reflow solder connections per	5.1.14-1
$\pi_{Ti} = \pi_{Qi} = 1$ as determined on	5.1.14
and so	
$\lambda_P = 2.1 * 121 * .000069 =$ **0.018 failures/million hours**	

The combined failure rate for all components is determined as shown in Table C5.

Table C5. Module Predicted Reliability

Four 256K CMOS SRAMs	4 * 1.81 = 7.24
One Decoder	1 * .279 = 0.279
One Set interconnects	1 * .018 = 0.018
Total	**7.537 failures/million hrs.**

This analysis indicates that the S128K8 has a calculated reliability of 3.605 failures/million hours and modules have 7.537 failures/million hours under these conditions. The importance of this is not the actual number, but the ratio between the two which will hold for any set of conditions. The memory portion of a system using S128K8s will be over twice as reliable as one using modules. If the system has a high memory content, this will be significant.

inova microelectronics

Application Note 3

NO-WAIT-STATE OPERATION for 25MHz 68020s & 68030s Using S128K8 SRAM

The S128K8, Inova's 1-megabit CMOS Static RAM, is an ideal part from which to construct No-Wait-State Memory for the MC68020 and MC68030 microprocessors. The S128K8 has 70 nanosecond access time, and only eight S128K8 devices are used per megabyte of memory. The most important feature of the devices, however, is that they are Static rather than Dynamic RAMs.

Dynamic RAMs may lose data when the clocks provided to them are too short. For most DRAMs, once clocks and enable inputs are asserted it is best to keep them asserted for a minimum time period. As a result a DRAM cycle should not be started unless it can be completed. Additionally, the address must be guaranteed stable at the leading edge of the RAS clock. To meet these requirements, DRAM cycles for the MC68020 and MC68030 should not be started until the CPU asserts Address Strobe.

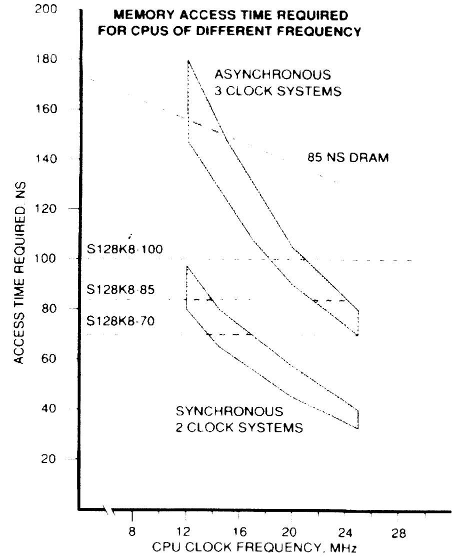
Since the S128K8 is a Static RAM, it can have its Enable inputs deasserted at any time without loss of data. This provides users the flexibility to enable the SRAM at the first hint that a cycle might take place on the bus. These enabling signals are then deasserted if the cycle is false. In addition to the flexible use of the Enables, Addresses are allowed to change after the Enable inputs are asserted. These features allow the S128K8 to be enabled using the External Cycle Start (ECS\) signal from the CPU. Since the ECS\ signal is asserted almost one clock prior to the AS\, this is a major factor in improving access time.

Static RAMs, unlike Dynamics, have no interfering refresh cycles, which introduce Wait States in microprocessor-based systems. Most SRAMs are also faster than DRAMs. The S128K8 has access times as fast as 70 nanoseconds which is satisfactory to allow asynchronous, No-Wait State operation in 25 MHz CPUs.

A curve of access time requirements versus clock frequency is shown in Figure 1. This graphically represents two and three cycle responses with access time requirements shown on the vertical axis.

This figure shows that 85 nanosecond SRAM devices can service 20 MHz processors and that 70 nanosecond devices are needed for 25 MHz CPUs. The penalty paid for the use of DRAMs is also shown. This penalty consists of 25-35 nanosecond refresh resolution time plus the percentage of one cycle from ECS\ to AS\.

Figure 1.



In Figure 2 we see a 2-megabyte, on-board, No-Wait State memory for an MC68020 microprocessor based system. The memory is constructed using four rows of four S128K8-70CC CMOS Static RAMs.. Each row represents 131,072 long words. Timing is shown in Figure 6.

All four rows of devices have Chip Select (CSx\) asserted by ECS\ as soon as it is available from the CPU. This increases array power but saves one wait state in every memory reference. Of course, one row must be selected and this is done with the Output Enable (OEx\). The Circuit for this is shown in Figure 3.

Figure 2

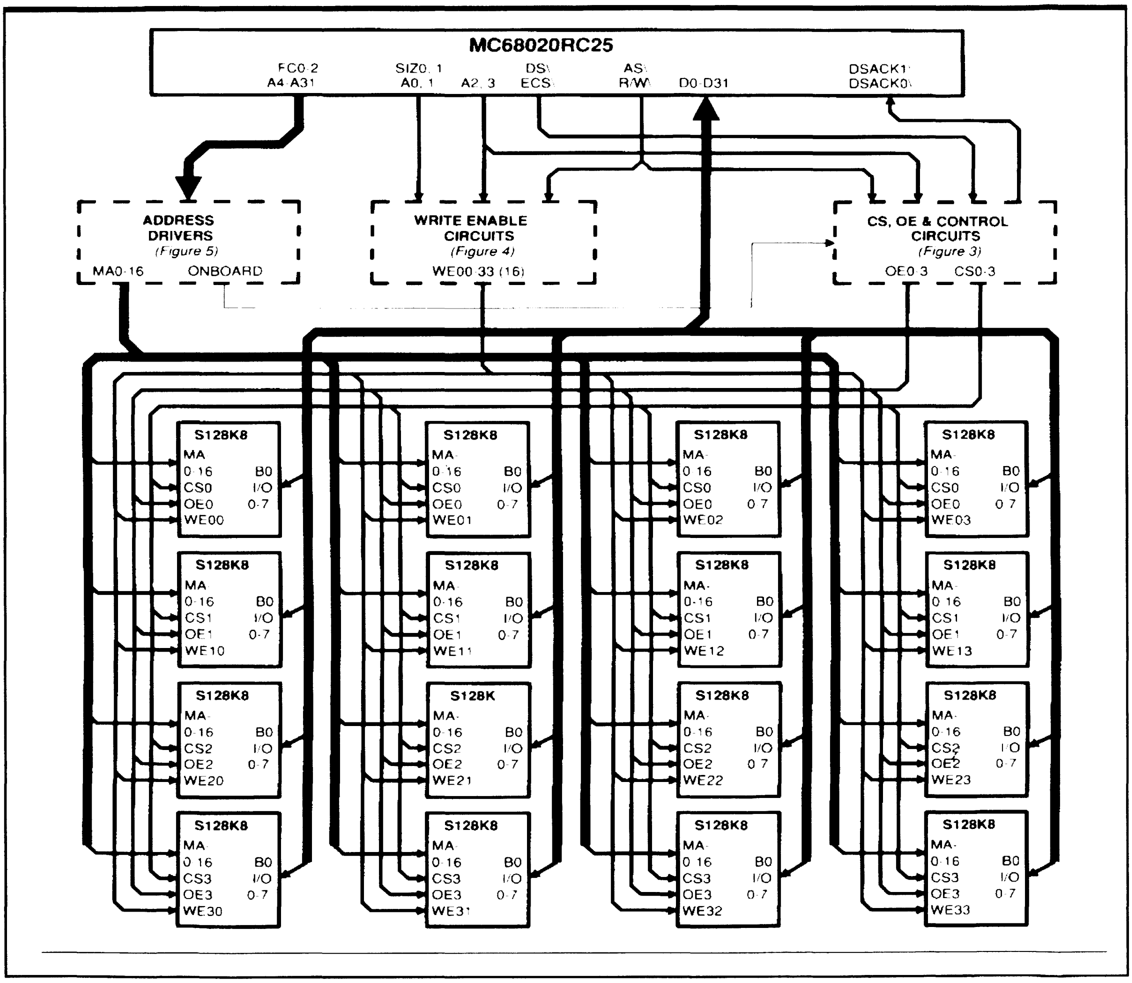


Figure 3 also shows the circuitry required to enable and read the device. In this implementation all four rows of Chip Selects are driven at once. When ECS\ is asserted by the CPU it performs two functions. First it directly supplies the leading edges of CS0\-CS3\ through the Negative-OR 74AS08. These outputs are capable of driving a 50 pF load in 5.5 nanoseconds worst case and each row has a typical load of only 20pF. The second function is to reset the latch which controls CS\ for the rest of the cycle.

The clock for this D-latch is CLK\, the inverse of the CPU clock. This causes the latch to change state on the falling edge of the CPU Clock. On the first falling edge of an external cycle ECS\ will be low resetting the D-latch and over-riding any clocked operation. At the second falling edge and every falling edge thereafter, the D-latch will assume the state of AS\ for the following cycle. If there was no bus cycle and no AS\ was ever asserted (as in the case of an internal cache hit) the circuit turns off on the falling edge of the S2 clock.

The circuit keeps Chip Enable asserted until a potential S0 clock following the present one. fIf an external cycle follows the present cycle the Chip Select remains low, as shown in Figure 6. As long as one cycle follows another the Chip Select stays low. Only when the following cycle is not an external bus cycle does the Chip Select go off. The 74AS74 is turned off when AS\ is high. The clock used is the inverse of the MC68020 clock. The CS\ signal will turn off at S3 if the cycle is in internal Cache and at S1 of the following cycle if that cycle is not an external bus cycle. If a series of external bus cycles are to be performed, the CS\ will remain asserted until the S1 clock of the cycle which follows the last external bus cycle.

If low operating power were a more critical requirement than chip count, qualification of the Address Strobe would be possible since the setup time requirement of the 74AS74 is 4.5 nanoseconds and the circuit as shown allows 22 nanoseconds.

Figure 3

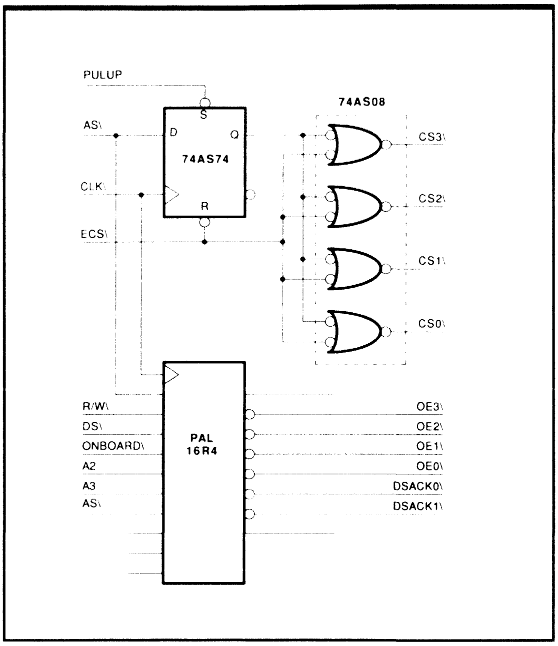


Figure 4

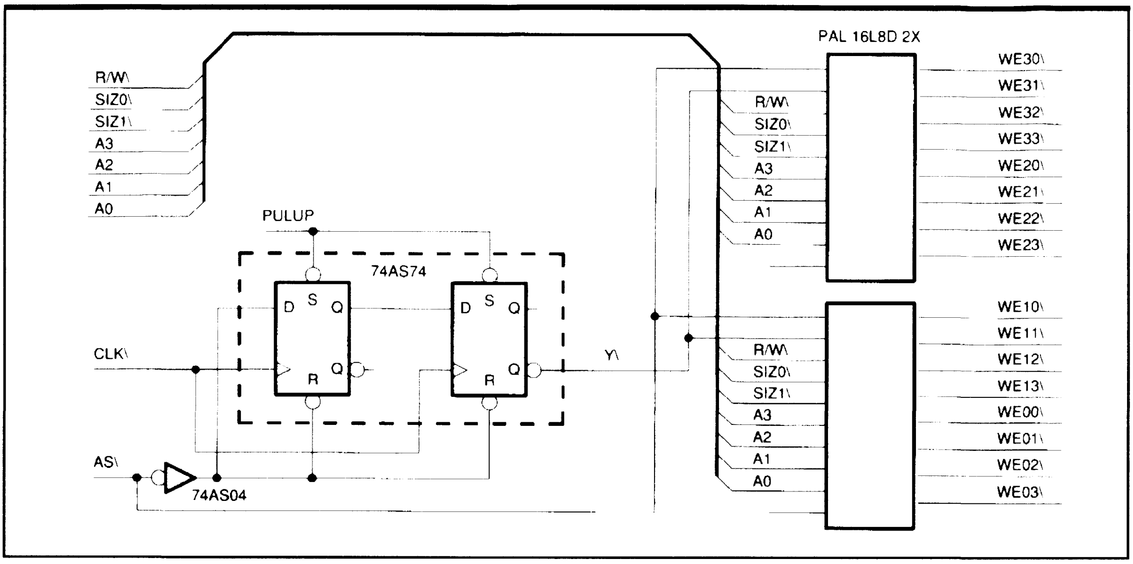


Figure 5

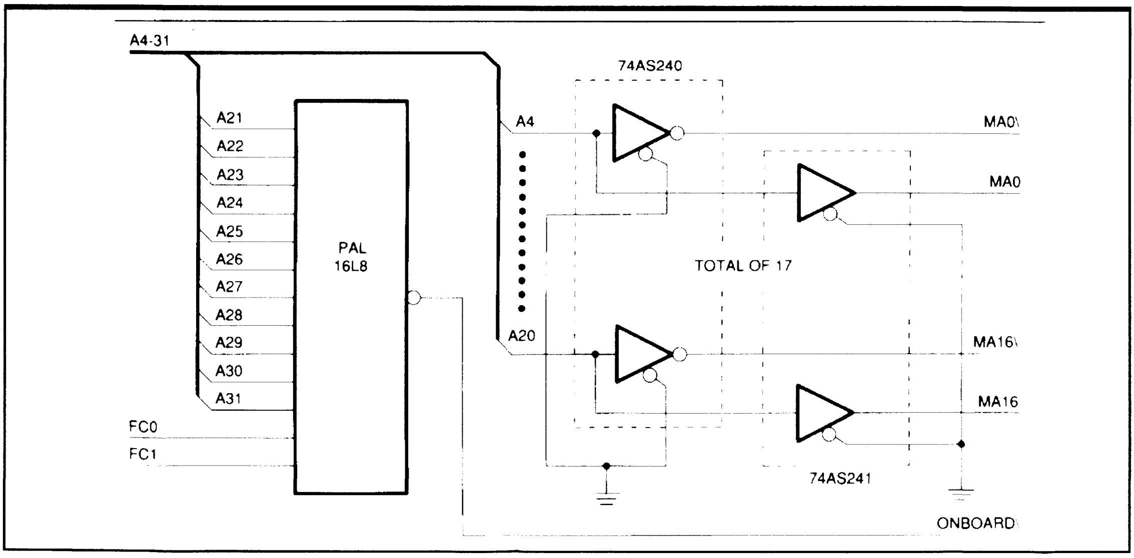
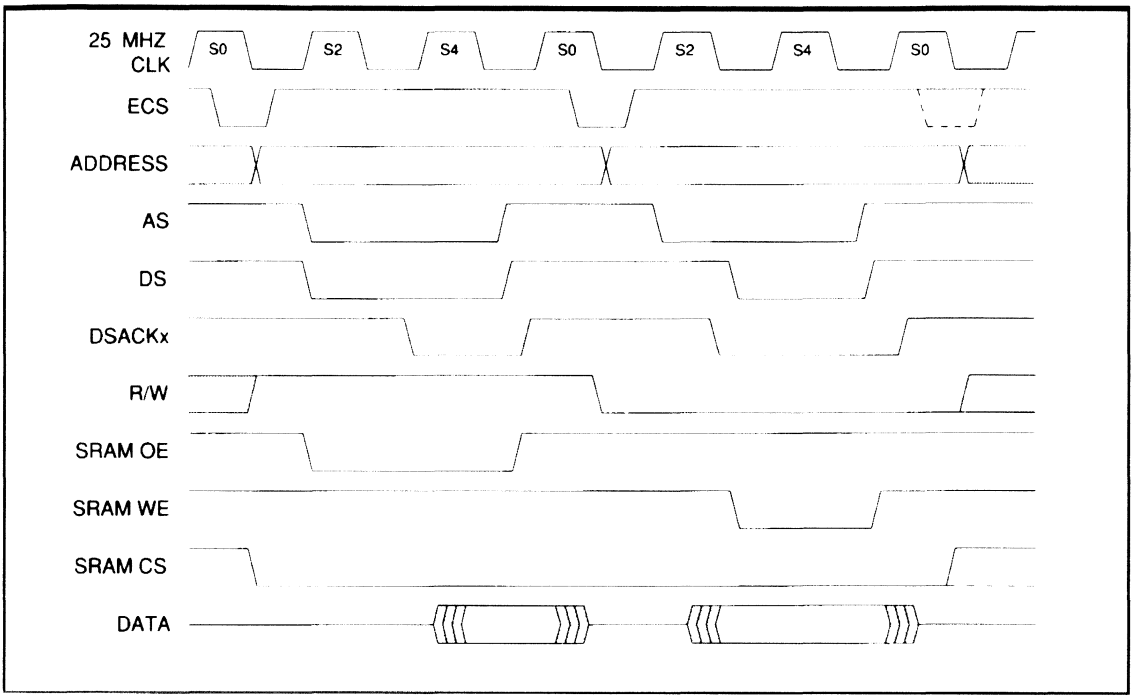


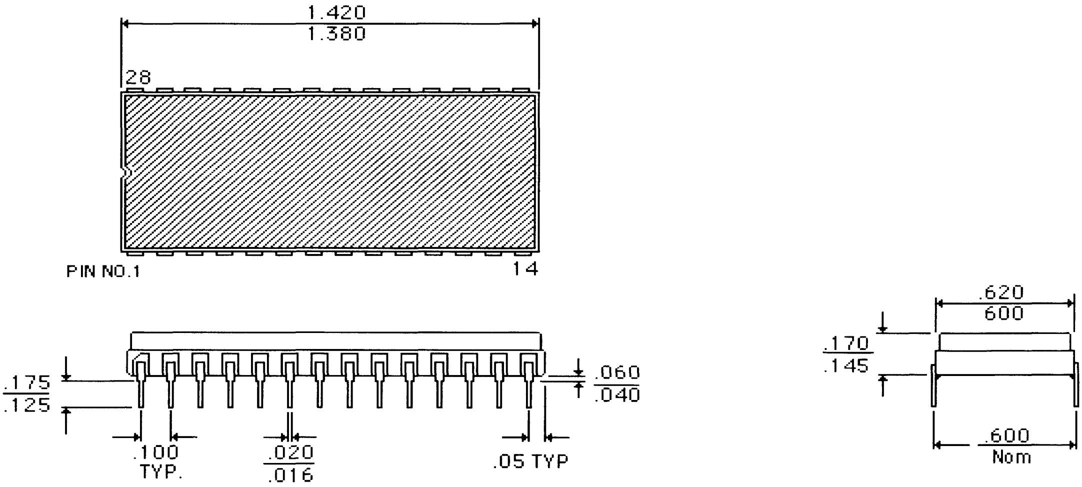
Figure 6


25 MHZ CLK
S0
S2
S4
S0
S2
S4
S0
ECS
ADDRESS
AS
DS
DSACKx
R/W
SRAM OE
SRAM WE
SRAM CS
DATA

Packaging

28 PIN CERAMIC SIDEBRAZED DUAL-IN-LINE PACKAGE 600 MILWIDE

C



32 PIN CERAMIC SIDEBRAZED DUAL-IN-LINE PACKAGE 600 MIL WIDE

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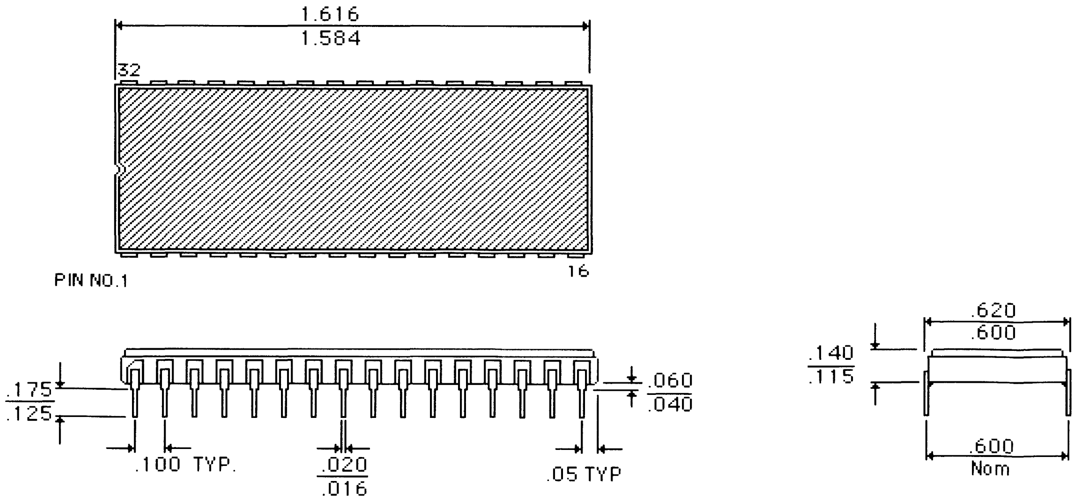

32 PIN CERAMIC SIDEBRAZED DUAL-IN-LINE PACKAGE 400 MIL WIDE

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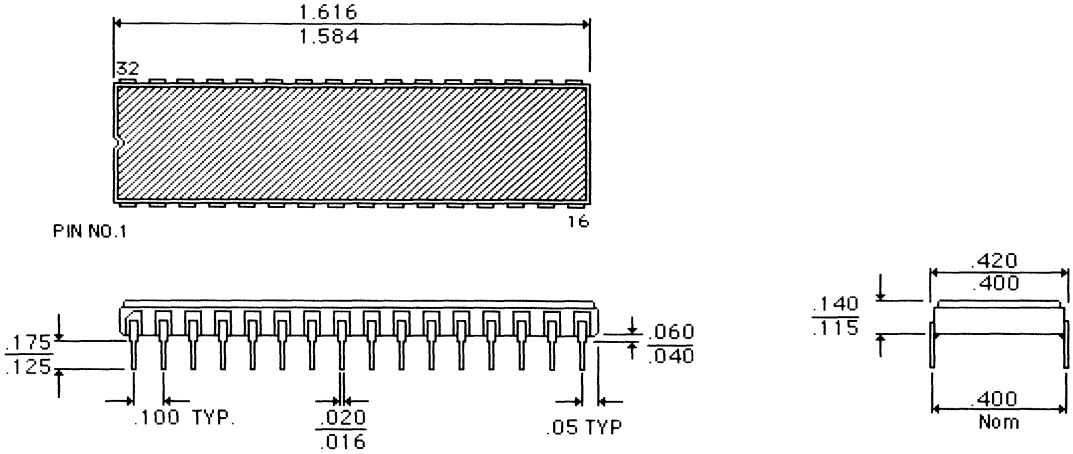

32 PIN CERAMIC SIDEBRAZED DUAL-IN-LINE PACKAGE 300 MIL WIDE

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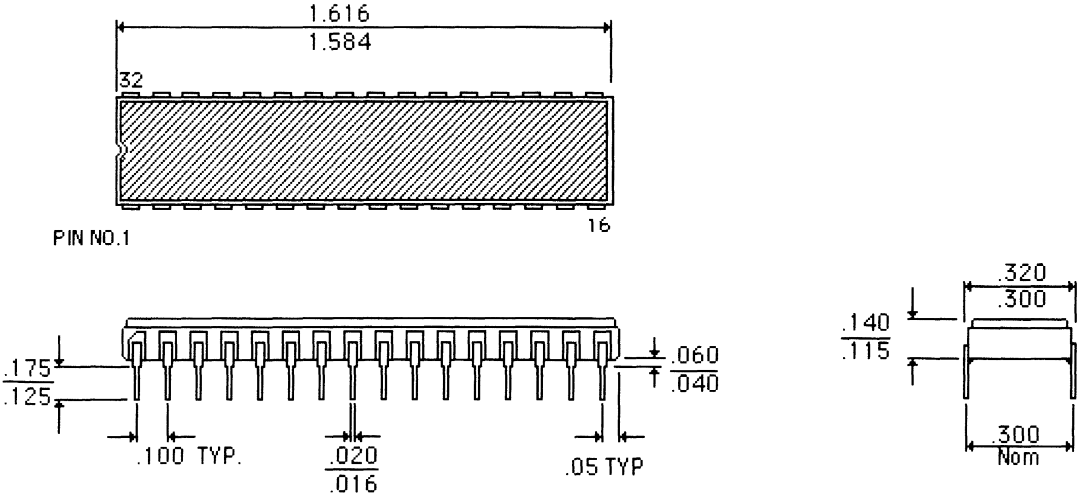
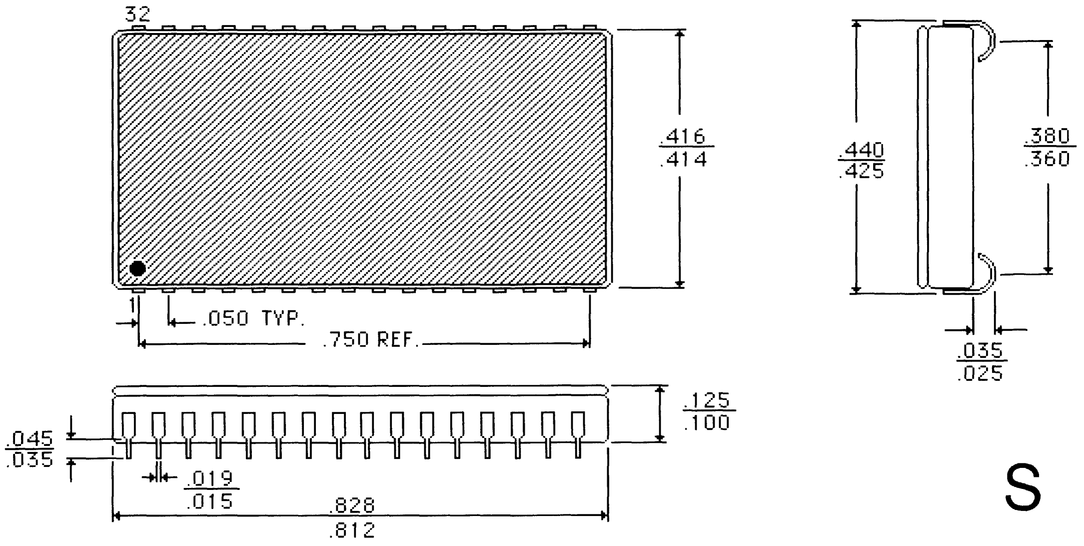
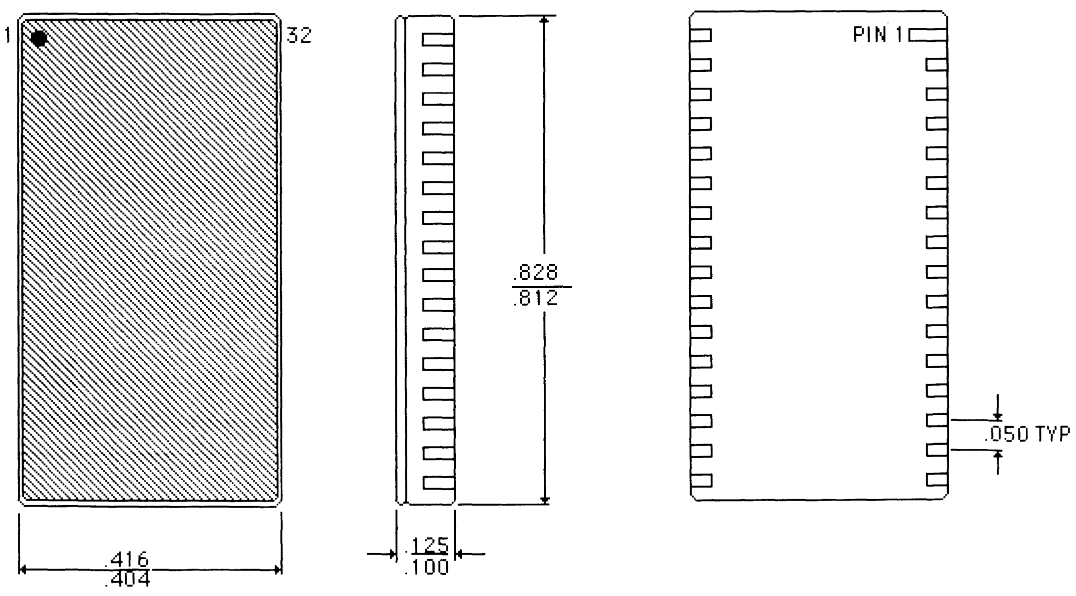


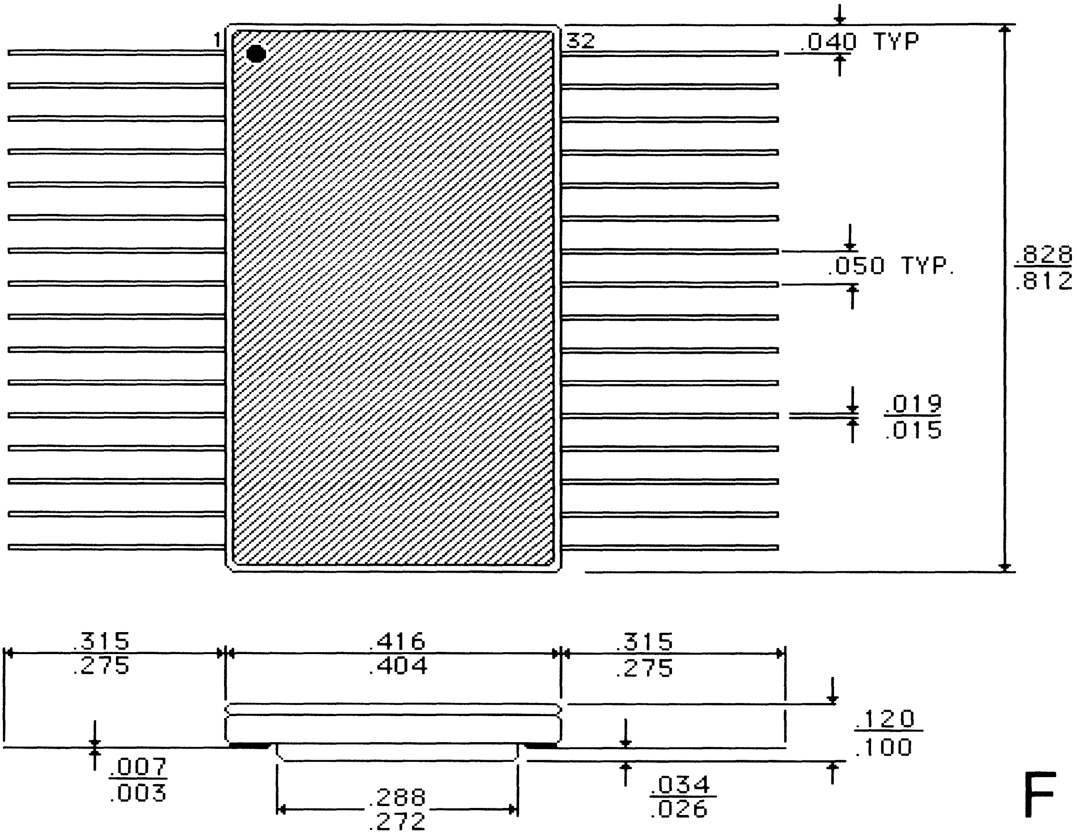
32 PIN CERAMIC "J" LEADED 400 MIL WIDE PACKAGE



32 PIN LEADLESS CHIP CARRIER PACKAGE



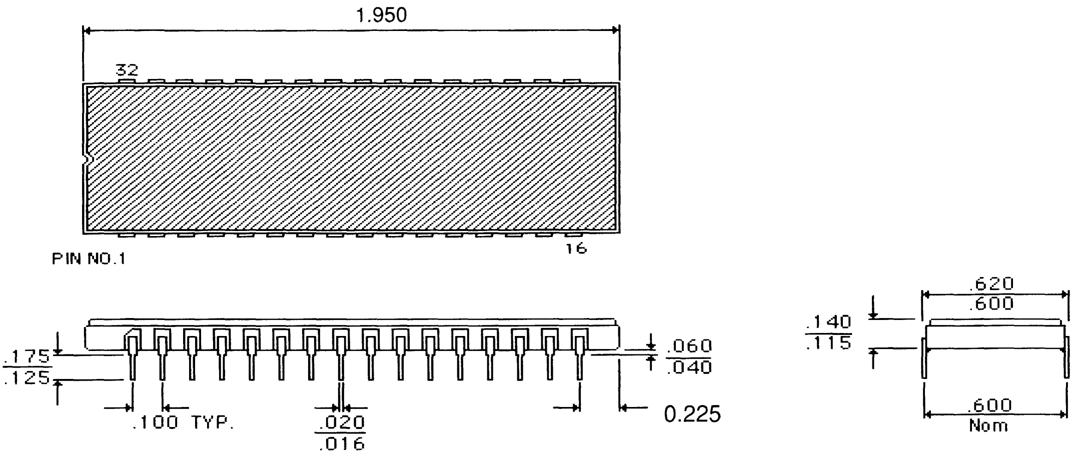
32 PIN CERAMIC FLATPACK,400 MIL WIDE PACKAGE



F

32 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
600 MIL WIDE

C



40 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
600 MIL WIDE

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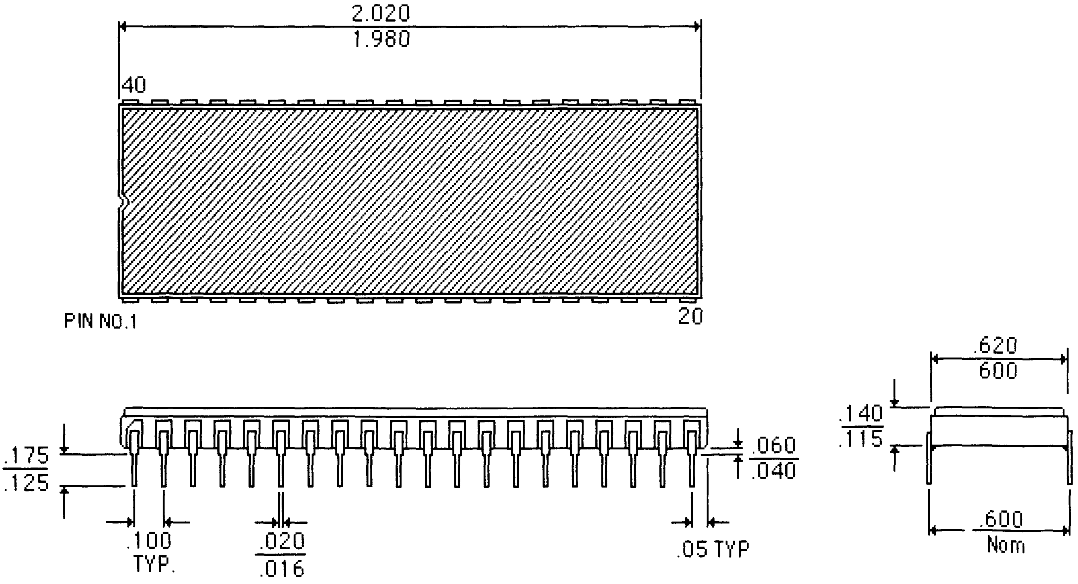
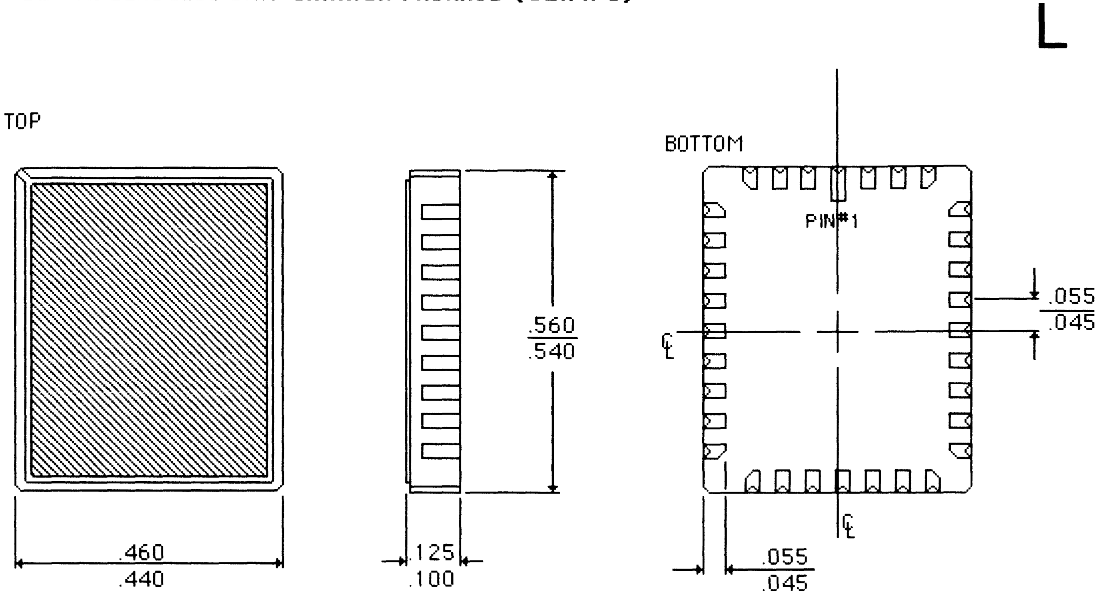
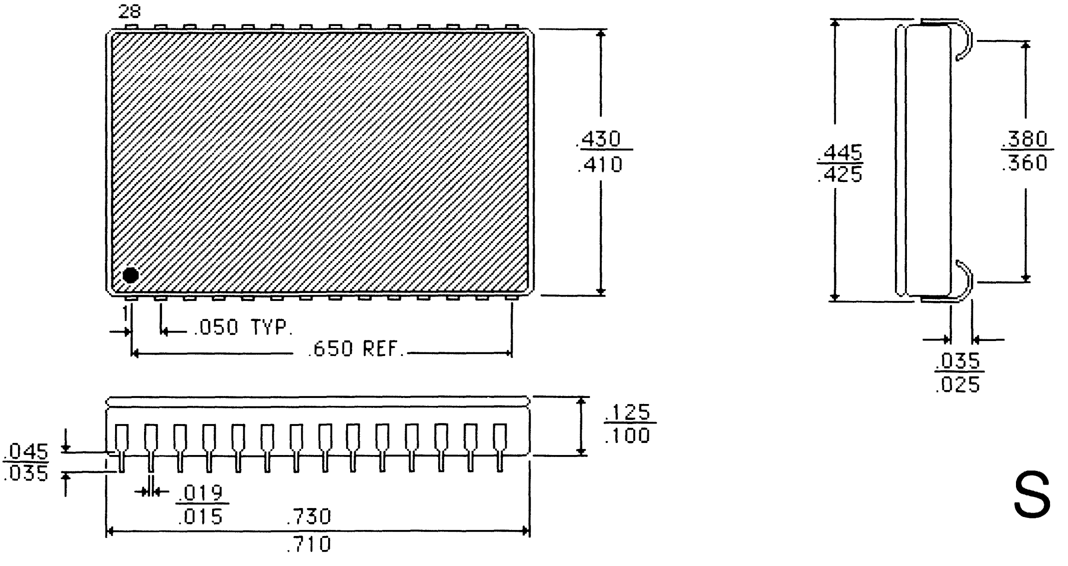


32 PIN LEADLESS CHIP CARRIER PACKAGE (32K X 8)



28 PIN CERAMIC "J" LEADED 400 MIL WIDE PACKAGE



32 LEAD (400 MIL) CERDIP PACKAGE

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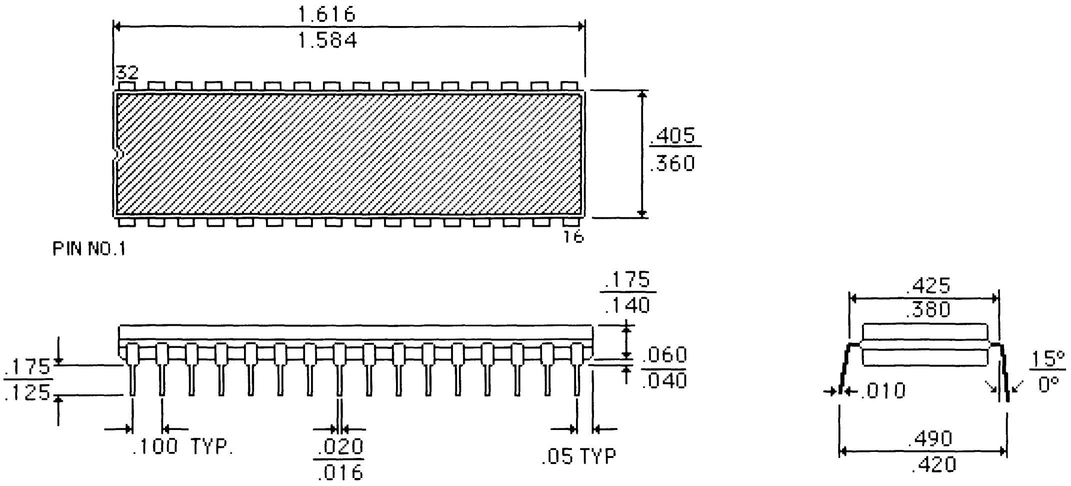

32 LEAD (400 MIL) MOLDED DIP PACKAGE

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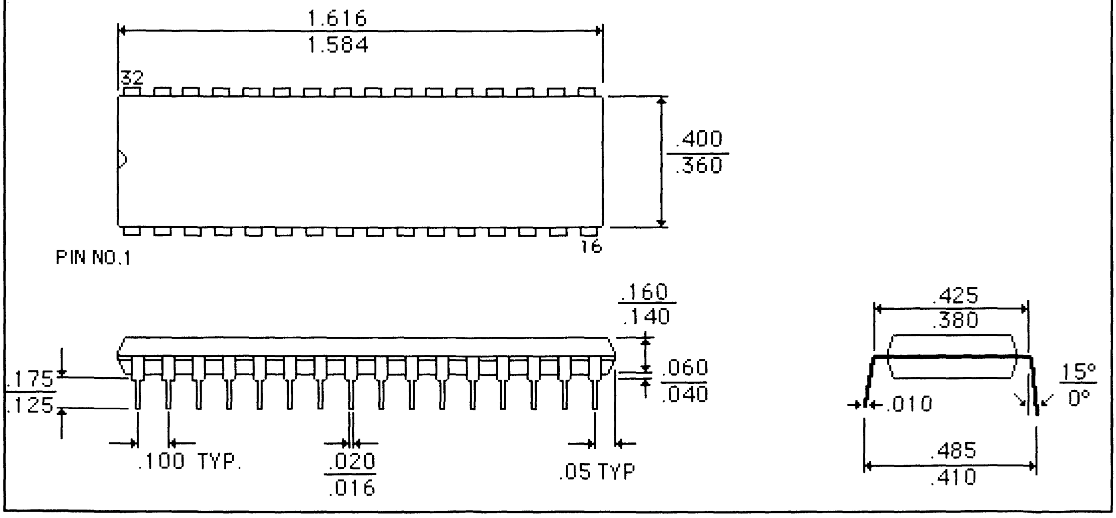
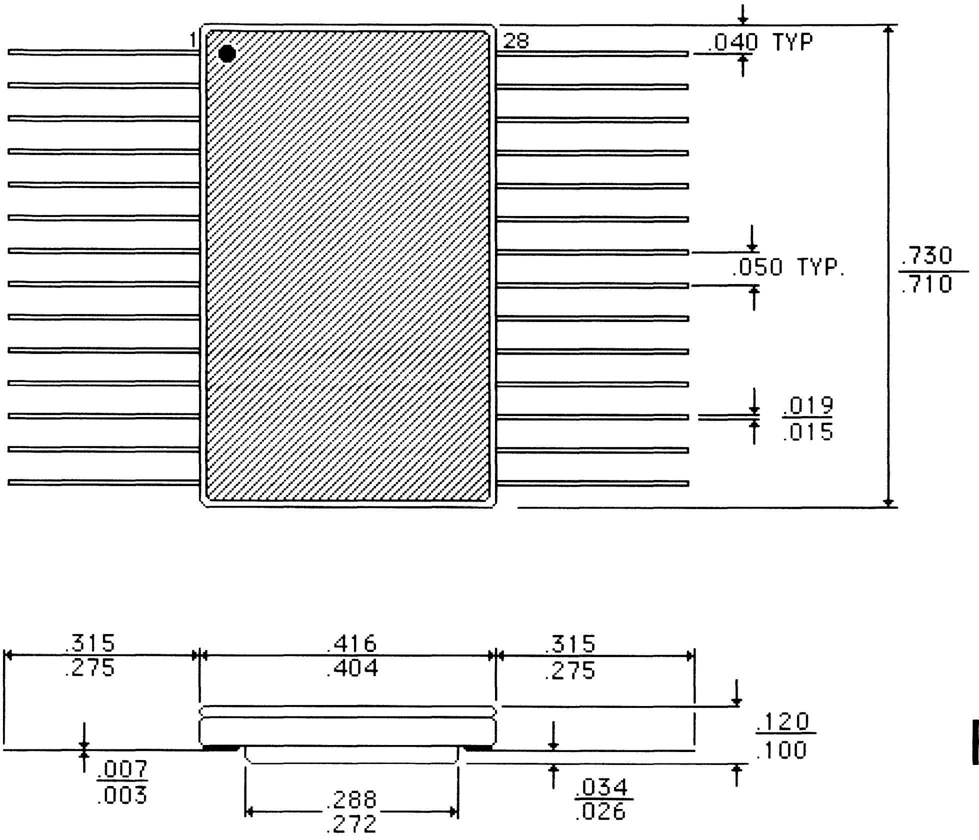


28 PIN CERAMIC FLATPACK,400 MIL WIDE PACKAGE



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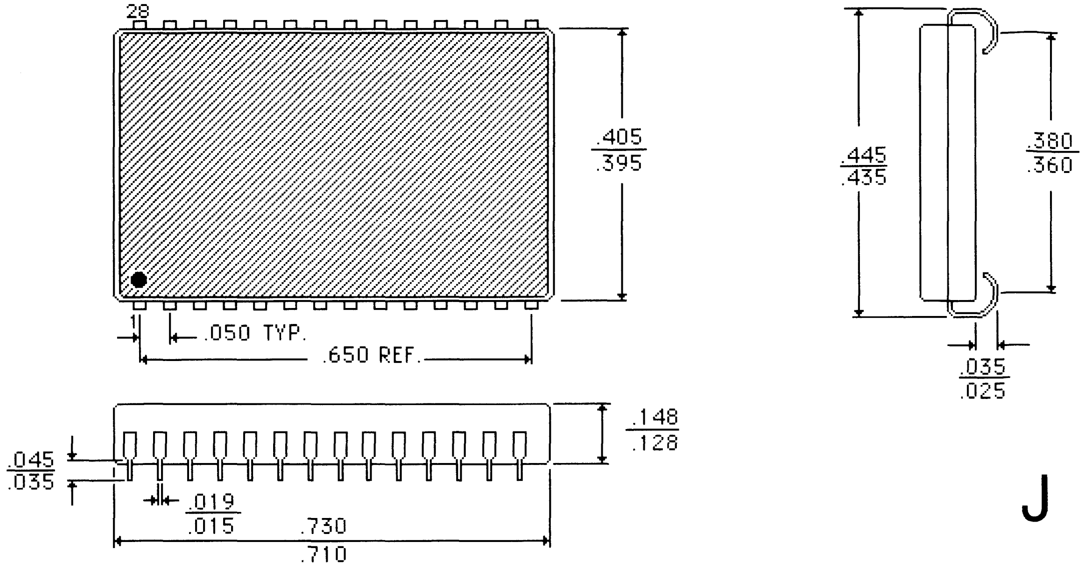
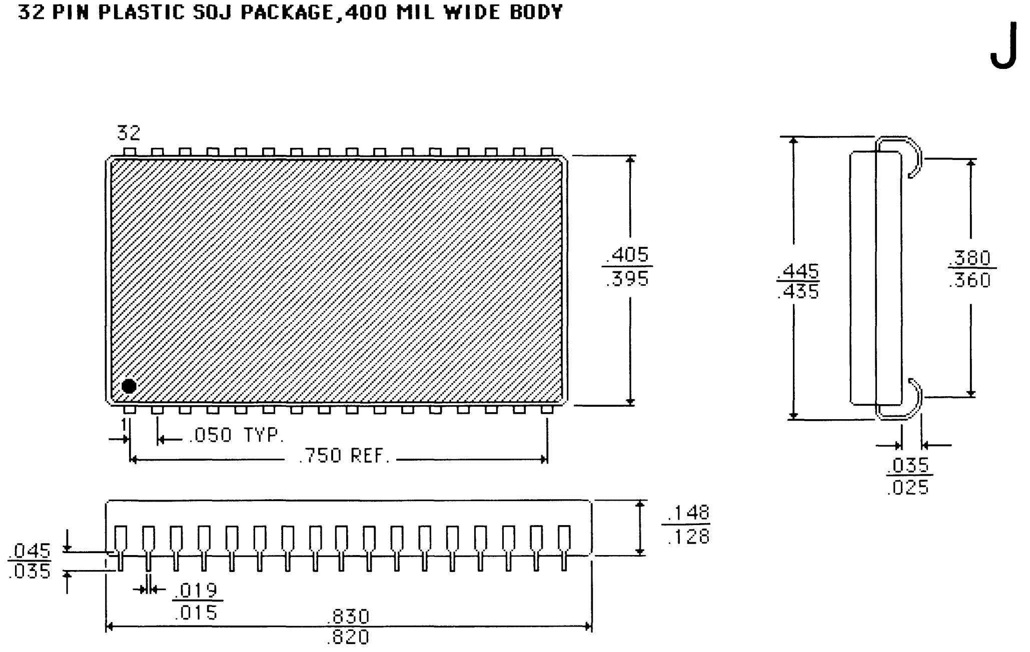
28 PIN PLASTIC SOJ PACKAGE,400 MIL WIDE BODY



32 PIN PLASTIC SOJ PACKAGE,400 MIL WIDE BODY



28 PIN CERAMIC SIDEBRAZED DUAL-IN-LINE PACKAGE 400 MIL WIDE

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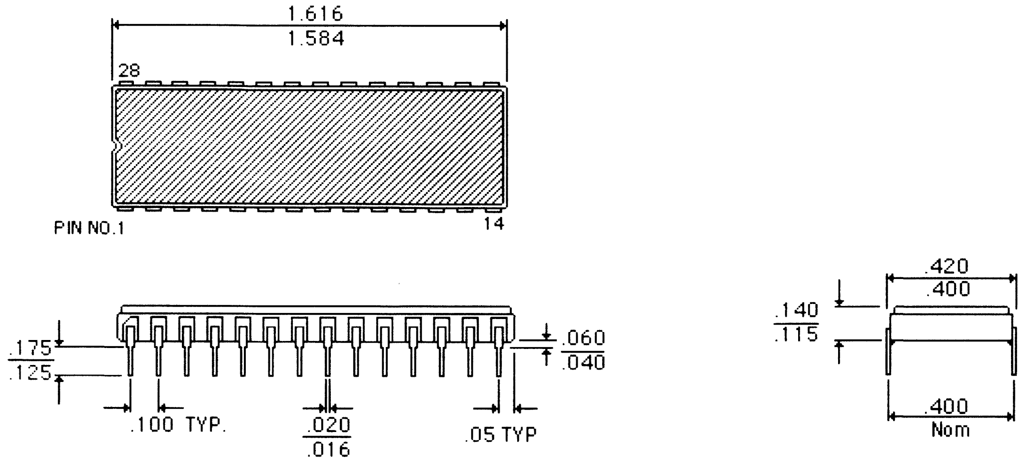

28 PIN CERAMIC SIDEBRAZED DUAL-IN-LINE PACKAGE 300 MIL WIDE

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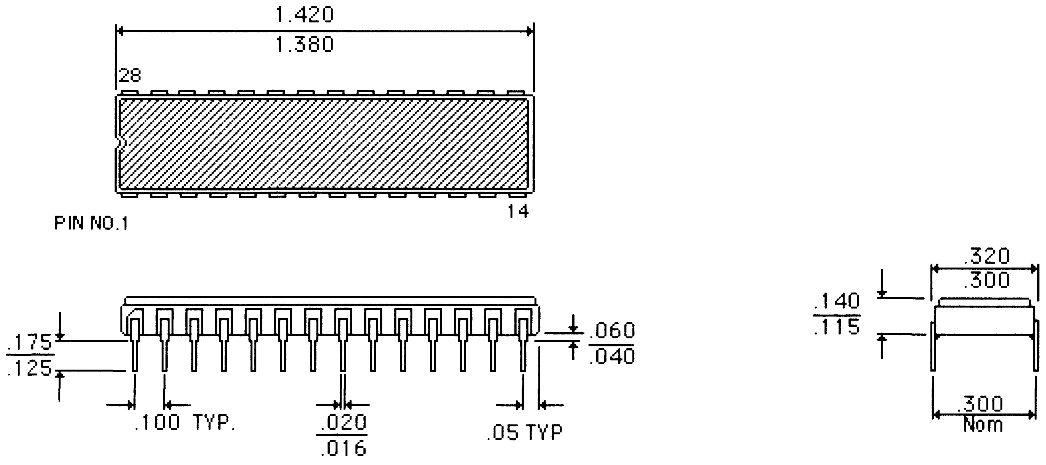

28 LEAD (400 MIL) CERDIP PACKAGE

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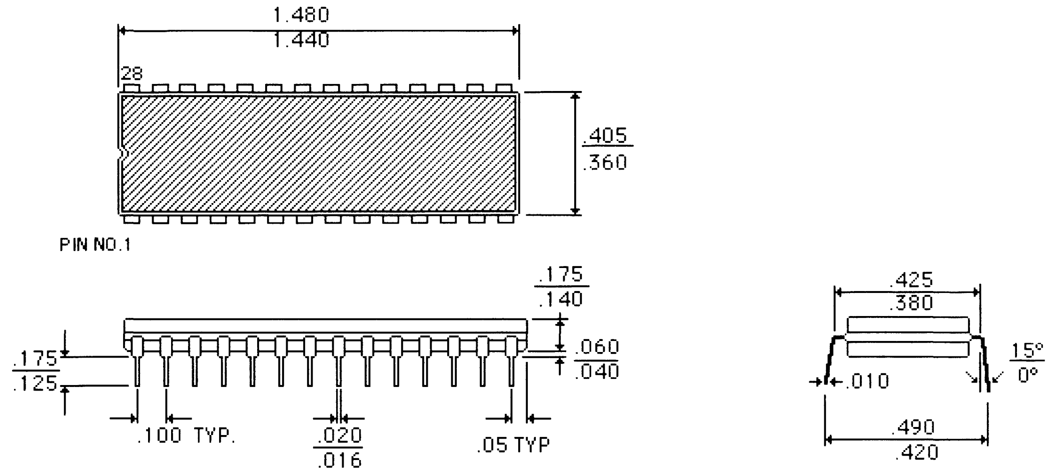

28 LEAD (400 MIL) MOLDED DIP PACKAGE

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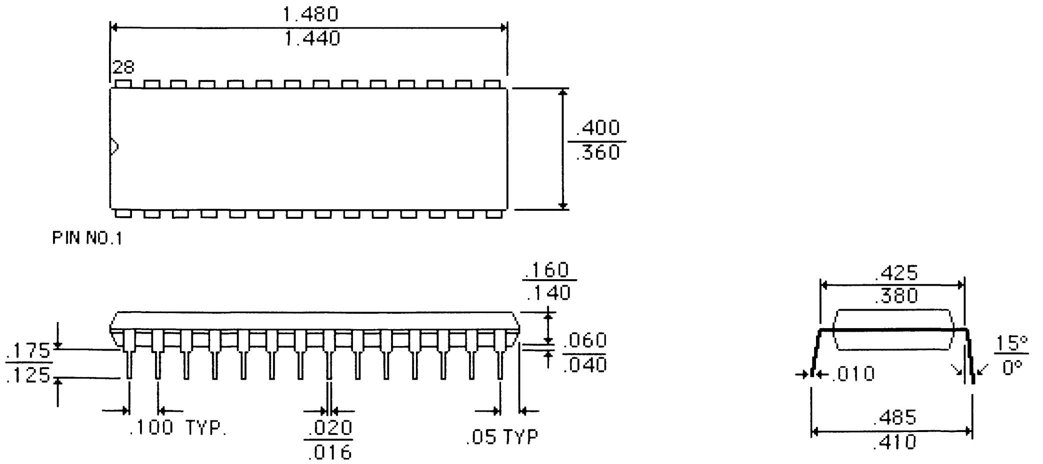

48 PIN CERAMIC SIDEBRAZED DUAL-IN-LINE PACKAGE 600 MIL WIDE

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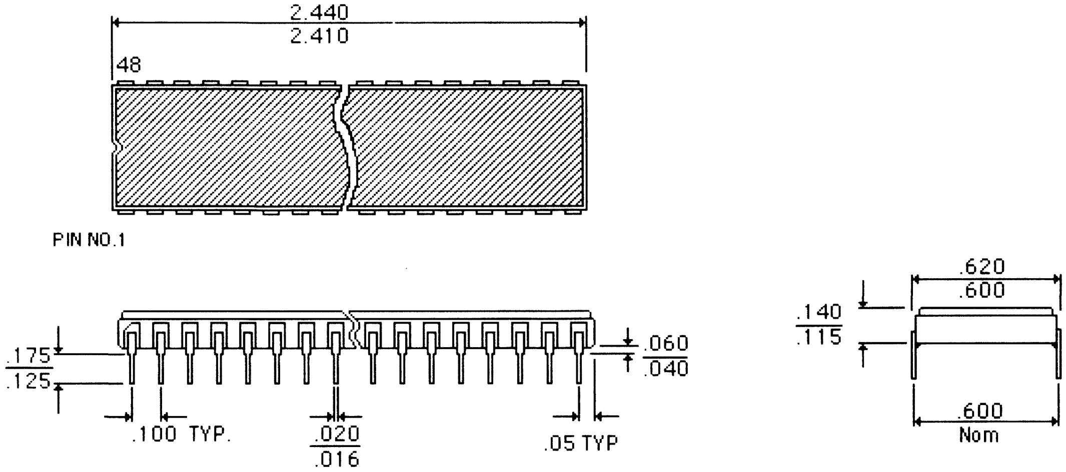
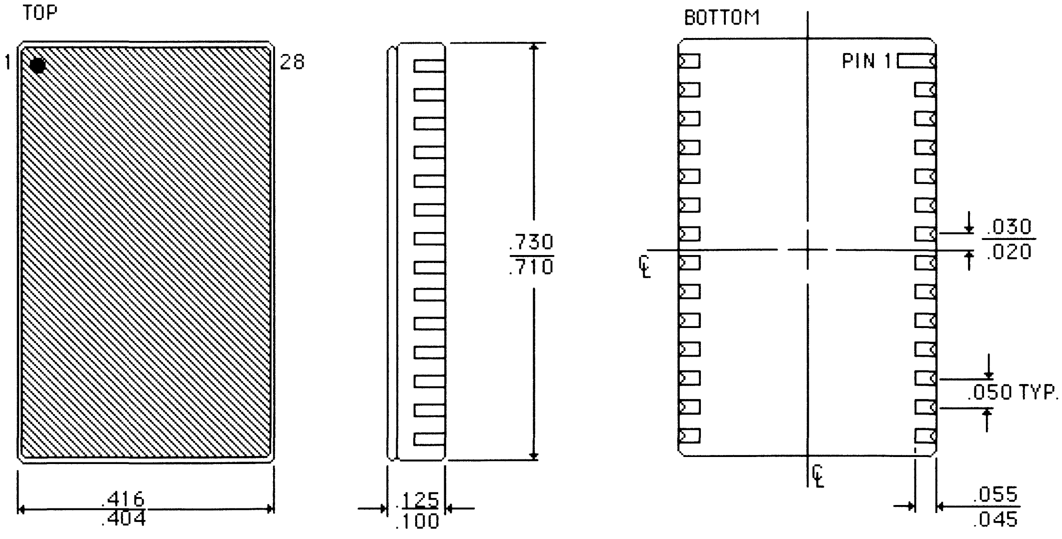


28 PIN LEADLESS CHIP CARRIER PACKAGE

L



209 PIN CERAMIC PIN GRID ARRAY PACKAGE

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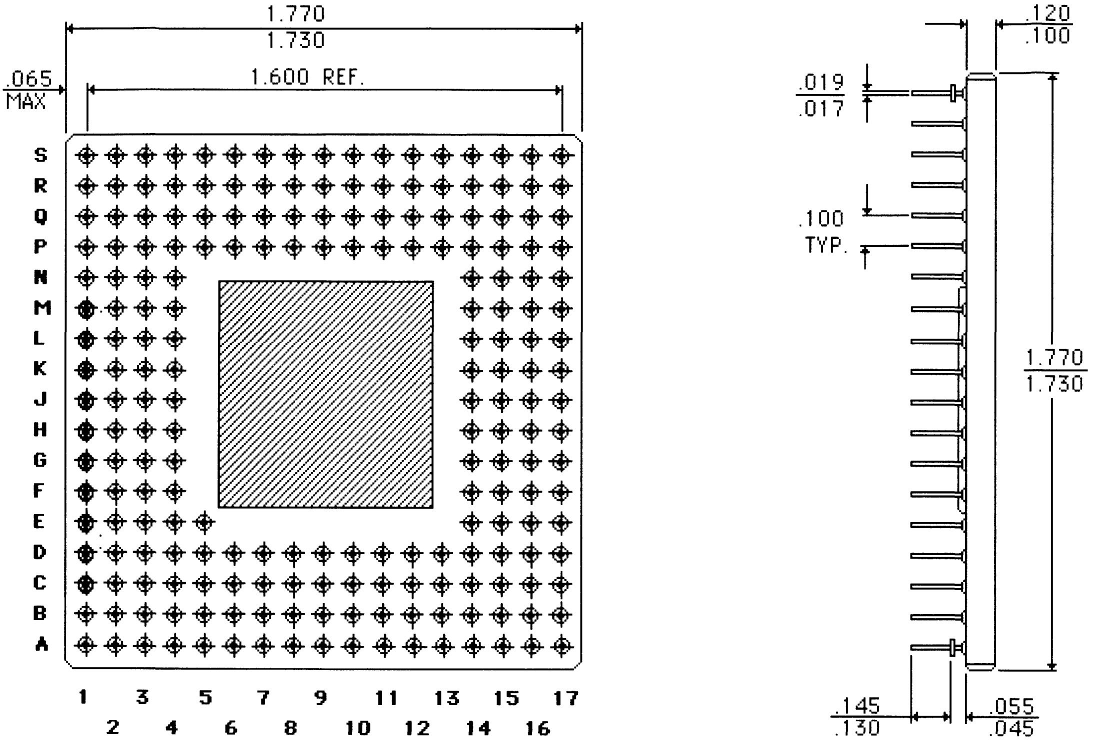

105 PIN CERAMIC PIN GRID ARRAY PACKAGE

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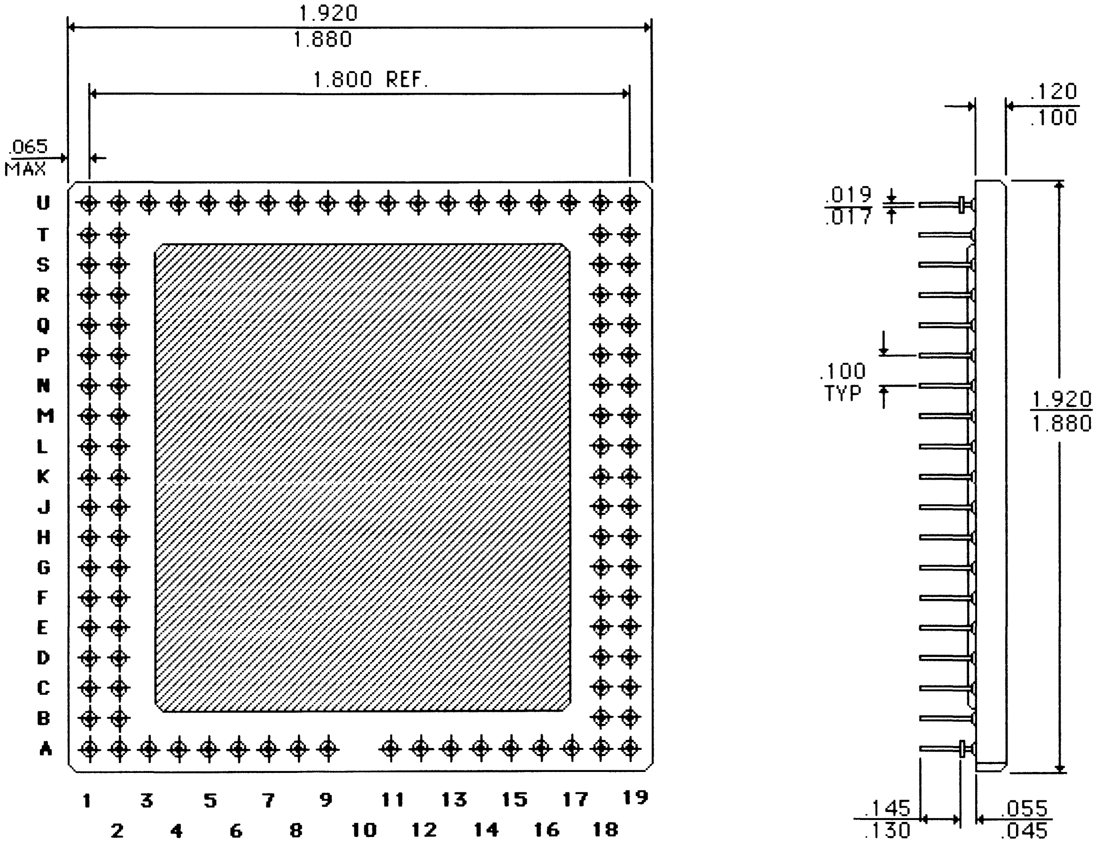
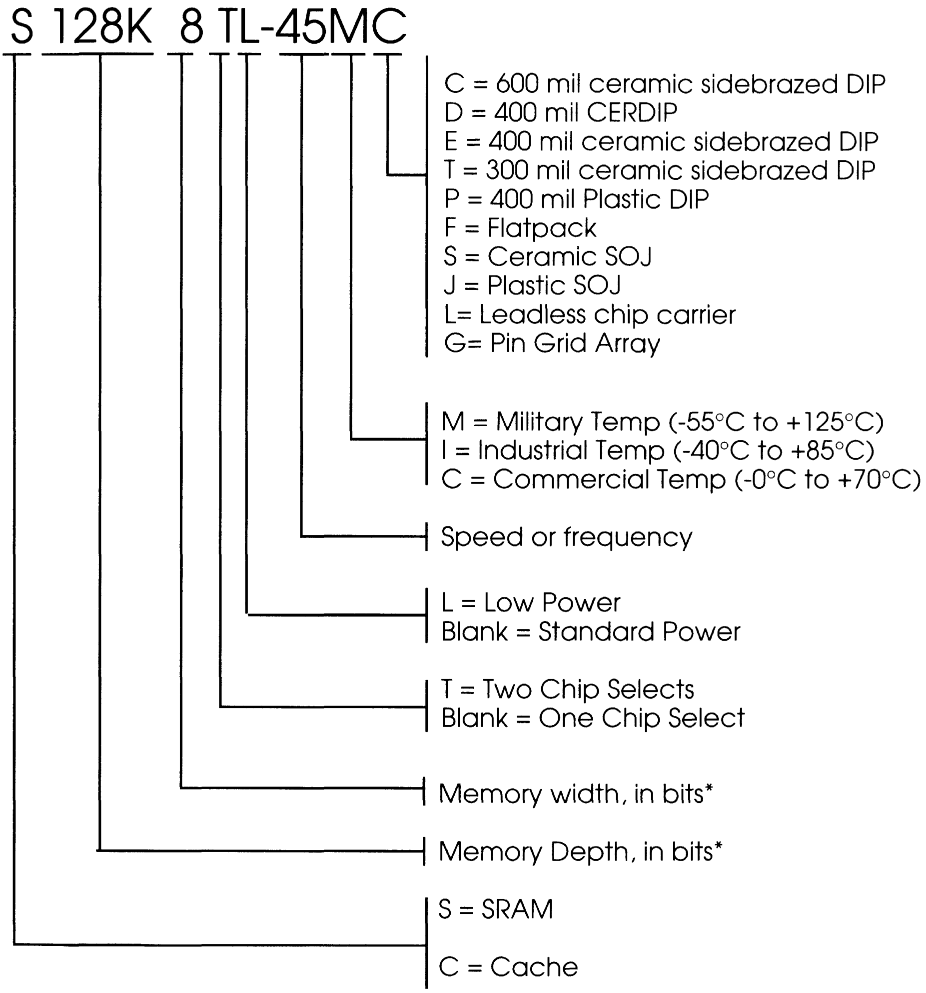


Ordering Information



S 128K 8 TL-45MC

C = 600 mil ceramic sidebrazed DIP
D = 400 mil CERDIP
E = 400 mil ceramic sidebrazed DIP
T = 300 mil ceramic sidebrazed DIP
P = 400 mil Plastic DIP
F = Flatpack
S = Ceramic SOJ
J = Plastic SOJ
L= Leadless chip carrier
G= Pin Grid Array

M = Military Temp (-55°C to +125°C)
I = Industrial Temp (-40°C to +85°C)
C = Commercial Temp (-0°C to +70°C)

Speed or frequency

L = Low Power
Blank = Standard Power

T = Two Chip Selects
Blank = One Chip Select

Memory width, in bits*

Memory Depth, in bits*

S = SRAM

C = Cache

*or another unique circuit designator

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